Low-T, High-κ Dielectrics for Transparent/Flexible 2D Electronics

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25 slides
Outline

• Introduction and Motivation
• Methodology
• Benchmark ALD Oxides
• Processing on PDMS
• Processing on PEN
• Conclusions and Future Work
Motivation – Transparent/Flexible 2D Oxides

- NEED: Low-T, high-κ, flexible-compatible, thin film oxides
Motivation – Transparent/Flexible 2D Oxides

- Y. Wu, S. Yu, and S. Li with J. Provine (EE 412, Fall 2010)

![Graphs showing comparison between Al₂O₃ and HfO₂](image-url)
Methodology – Process Flow

1. Clean SiO$_2$/Si
2. Ti/Au deposition
3. Oxide anneal
4. High-κ layer deposition
5. ALD oxide deposition
6. Top electrode deposition
Methodology – Measurements

- All caps were measured from 0 → 1 → -1 → 0 V.
- Capacitances changed by <1% over this range.
- A line was fit to the data, with the slope being the “skew” and the C-V intercept value taken for fitting C/A.
Methodology – Capacitor “TLM” Arrays

We can do the same thing with capacitors!

AFM

We can do the same thing with capacitors!
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Savannah - 150 °C Alumina + 200 °C FGA

- $C = 0.716 \pm 0.009$
- $0.713 \pm 0.006 \ \mu F/cm^2$
- $R^2 = 1.000, 1.000$
- $d = 9.4 \ \text{nm}$
- $\kappa = 7.60 \pm 0.10, 7.56 \pm 0.06$

$C$ vs. $A$

- parasitic $C$
- $\sim 10 \ \text{nm} \ \text{Al}_2\text{O}_3$
- $\sim 7 \ \text{nm} \ \text{SiO}_2$
- Ti/Au
- Ti/Au
- p++ Si

$I_{\text{Leak}}$ vs. $V_{\text{DC}}$

- $I_{\text{Leak}} < \text{nA}$
- $V_{\text{BD,soft}} \sim 3.0 \ \text{V}$
- $E_{\text{crit,soft}} \sim 0.32 \ \text{V/nm}$
- $V_{\text{BD,hard}} > 7.0 \ \text{V}$
- $E_{\text{crit,hard}} \sim 0.74 \ \text{V/nm}$
Savannah - 150 °C Hafnia + 200 °C FGA

C vs. A

- $C = 1.39 \pm 0.02$
- $1.38 \pm 0.01 \, \mu F/cm^2$
- $R^2 = 1.000, 1.000$
- $d = 10.5 \, nm$
- $\kappa = 16.5 \pm 0.3, 16.3 \pm 0.1$

$I_{\text{Leak}}$ vs. $V_{\text{DC}}$

- $I_{\text{Leak}} < nA$
- $V_{\text{BD}} > 4.5 \, V$
- $E_{\text{crit}} \sim 0.43 \, V/nm$
MVD - 125 °C Hafnia + 125 °C FGA

C vs. A

- $C = 1.57(4) \pm 0.004$
- $1.56(6) \pm 0.004 \mu F/cm^2$
- $R^2 = 1.000, 1.000$
- $d \approx 11.2 \text{ nm}$
- $\kappa \approx 15.9 \pm 0.1, 15.8 \pm 0.1$

no parasitic C

$\sim 10 \text{ nm HfO}_2$

$I_{\text{Leak}}$ vs. $V_{\text{DC}}$

- $I_{\text{Leak}} < nA$
- $V_{\text{BD}} > 5.5 \text{ V}$
- $E_{\text{crit}} \sim 0.49 \text{ V/nm}$
Results – Benchmark ALD Oxides on SiO₂

- Savannah and MVD oxides are quite similar.
- Al₂O₃ and HfO₂ show opposite trends in thickness, capacitance, and breakdown at lower temperatures.
- HfO₂ seems to be a considerably more stable process at low T.
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### Overview – Processing on Flexibles

<table>
<thead>
<tr>
<th></th>
<th>Hotplate Curing</th>
<th>Ovens $\geq 150 , ^\circ C$</th>
<th>Direct SPR 3612</th>
<th>Oxide/Metal Cracking</th>
<th>Thermal Wrinkling</th>
<th>Trivial Alignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$/Si</td>
<td>yes ✔️</td>
<td>yes ✔️</td>
<td>yes ✔️</td>
<td>no ✔️</td>
<td>no ✔️</td>
<td>yes ✔️</td>
</tr>
<tr>
<td>PDMS</td>
<td>no ✗</td>
<td>no ✗</td>
<td>no ✗</td>
<td>yes ✗</td>
<td>yes ✗</td>
<td>yes ✔️</td>
</tr>
<tr>
<td>PEN</td>
<td>yes ✔️</td>
<td>no ✗</td>
<td>?</td>
<td>no ✔️</td>
<td>no ✔️</td>
<td>no ✗</td>
</tr>
</tbody>
</table>

- Spoiler: PEN is easier to work with as a substrate than PDMS
Initial Cap Pads on PDMS

- PDMS thoroughly outgassed for 2 hours in vacuum and baked at 80 °C for 2 hours in ambient oven.
- PMGI (liftoff layer) baked on at 200 °C for 5 minutes
- Strong temperature gradient caused visible wrinkles near edges
- SPR 3612 baked in 90 °C oven for 25 minutes
- ~1 cm² in center of 2×2 cm chip had bubbles but no wrinkles
Cap Pads on PDMS – 2\textsuperscript{nd} Try

- PMGI spun on at 3000 rpm
- 230 °C bake in white oven for 25 mins (+ SPR 3612 and develop)
Cap Pads on PDMS – 3\textsuperscript{rd} Try

- PMGI spun on at 3000 rpm
- 150 °C bake in white oven (25 mins) or on hot plate (10 mins)
Cap Pads on PDMS – 4th Try

- No LOR – only SPR 3612 + 25 min bake in 90 °C oven
- Resist did not adhere well to PDMS – will need HMDS treatment
Photoresist and PDMS

- HMDS does not help with resist adhesion to PDMS.
- Deposited 100 cycles of ALD oxides prior to lithography.
- SPR 3612 much easier to spin on (without HMDS) to PDMS/high-κ.
- Possible alternative: spin on LOR and bake in the White oven at 100 °C for at least 4 hours before continuing with SPR 3612 and lithography.
• Wrinkles visible on metal for 150 °C oxides.
• Also happens for 125 and 100 °C oxides.

150 °C: PDMS/Al₂O₃/Ti/Au/Al₂O₃

150 °C: PDMS/HfO₂/Ti/Au post-liftoff
Cap Pads on PEN (polyethylene naphthalate)

- PMGI spun on at 3000 rpm + 150 °C bake on hot plate (10 mins)
- SPR 3612 spun on at 5000 rpm + 90 °C bake on hot plate
Caps on PEN – 100 °C MVD Oxides

- No cracks after metallization!
- Similar to PDMS, Au did not stick to Ti.
10 mins on 150 °C hotplate is fine, but an hour at 150 °C in the MVD causes plastic deformation of PEN. The Headway is consequently unable to achieve vacuum. Resist gluing and kapton tape do not work to fasten it to a carrier wafer.

ALD oxides deposited at 125 °C cause some bending, but substrates are still spinnable in the Headway. Alignment is very tricky, however. A quartz suppression wafer will be used in the future.
Films of any kind on PDMS do not fare well above 100 °C.

An initial layer of high-κ oxide is essential for resist adhesion, and helps prevent crud from sticking to the surface.

It is beneficial to forgo LOR and sonicate during liftoff to minimize the thermal budget.

Optical resist must be cured in the 90 °C oven.

PDMS is a sub-optimal substrate for device processing.

PEN acquires an irreversible bend if processed for long at elevated temperatures (≥150 °C), but remains flat at 125 °C.

Off-the-shelf PEN is very dirty, rough, and has scars. Microelectronics grade PEN is recommended for devices.

PEN is much more robust to thermal expansion and processing abuse than PDMS.
Conclusions and Future Work

Observations

- Savannah and MVD oxides show very similar characteristics.
- ALD $\text{Al}_2\text{O}_3$ ($\text{HfO}_2$) is a stable process down to 125 °C (100 °C).
- PDMS is very tricky for lithography due to stickiness, thermal expansion, and hydrophobicity.
- PEN is an alternative substrate that is much easier to work with.

Immediate Future Work

- Order microelectronics grade PEN.
- Fabricate caps with 125 °C oxides in MVD.
- Continue to smooth out processing issues.
Thanks for listening!

Many thanks are due to Dr. Howe, Dr. Rincon, and Dr. Chen for training, guidance, and support!
Backup Slides
Process Flow - Details

• Begin with clean SiO$_2$/Si wafer pieces

Lithography:
• PMGI SF6 @ 3000 rpm for 60 seconds + hotplate
• SPR 3612 @ 5000 rpm for 40 seconds + 90 °C hotplate
• Define bottom electrode with KarlSuss
• Develop for 45 seconds

Metallization:
• Ebeam evaporate 2/38 nm Ti/Au
• Soak in Remover PG for 3 hours
• Spray with acetone, IPA
• Sonicate if necessary
Process Flow - Details

• Precondition ALD chamber with recipe to be used
• \( \text{O}_2 \) plasma in MRC: 20 mTorr, 20 sccm, 50 W, 2 mins
• Immediately transfer chips to ALD chamber, deposit oxide
• FGA in AllWin_r and fit thickness with Woollam

• Repeat lithography for top electrode
• Repeat metallization for top electrode
• Measure devices
C vs. A
- $C = 0.703 \pm 0.060$
- $0.677 \pm 0.037 \ \mu F/cm^2$
- $R^2 = 0.998, 0.998$
- $d = 10.0 \ \text{nm}$
- $\kappa = 7.94 \pm 0.68, 7.65 \pm 0.42$

note: $\kappa$ values change by $<1\%$ for $\pm 1 \ V_{\text{DC}}$

$I_{\text{Leak}}$ vs. $V_{\text{DC}}$
- $I_{\text{Leak}} \sim nA$
- $V_{\text{BD,soft}} \sim 3.5 \ V$
- $E_{\text{crit,hard}} \sim 0.35 \ V/nm$
- $V_{\text{BD,soft}} \sim 7.5 \ V$
- $E_{\text{crit,soft}} \sim 0.75 \ V/nm$
Savannah - 200 °C Alumina, O₂ anneal

C vs. A

- C = 0.662 ± 0.021
- 0.679 ± 0.009 µF/cm²
- R² = 0.999, 1.000
- d = 10.0 nm
- κ = 7.48 ± 0.23, 7.67 ± 0.10

I_{Leak} vs. V_{DC}

- I_{Leak} ~ nA
- V_{BD,soft} ~ 3.5 V
- E_{crit,hard} ~ 0.35 V/nm
- V_{BD,soft} ~ 7.8 V
- E_{crit,soft} ~ 0.78 V/nm
Savannah - 200 °C Hafnia, FGA

**C vs. A**

- $C = 1.60 \pm 0.007$
- $1.61 \pm 0.004 \, \mu F/cm^2$
- $R^2 = 1.000, \ 1.000$
- $d = 8.7 \, \text{nm}$
- $\kappa = 15.70 \pm 0.07, \ 15.84 \pm 0.04$

**$I_{\text{Leak}}$ vs. $V_{\text{DC}}$**

- $I_{\text{Leak}} \sim \text{nA}$
- $V_{\text{BD}} \sim 3.2 \, \text{V}$
- $E_{\text{crit}} \sim 0.37 \, \text{V/nm}$

breakdown
Savannah - 200 °C Hafnia, O₂ anneal

**C vs. A**

- \( C = 1.59 \pm 0.011 \)
- \( 1.42 \pm 0.014 \ \mu F/cm^2 \)
- \( R^2 = 1.000, 1.000 \)
- \( d = 8.7 \ \text{nm} \)
- \( \kappa = 15.59 \pm 0.11, 13.95 \pm 0.14 \)

**I_{Leak} vs. V_{DC}**

- \( I_{Leak} \sim \text{nA} \)
- \( V_{BD} \sim 3.2 \ \text{V} \)
- \( E_{crit} \sim 0.37 \ \text{V/nm} \)
Savannah - 100 °C Hafnia, 150 °C FGA

**C vs. A**

- $C = 1.20 \pm 0.03$
- $1.10 \pm 0.01 \ \mu F/cm^2$
- $R^2 = 1.000, 1.000$
- $d = 11.9 \ \text{nm}$
- $\kappa = 16.2 \pm 0.4, 14.8 \pm 0.1$

**$I_{\text{Leak}}$ vs. $V_{\text{DC}}$**

- $I_{\text{Leak}} \sim \text{nA}$
- $V_{\text{BD}} > 6.0 \ \text{V}$
- $E_{\text{crit}} \sim 0.50 \ \text{V/nm}$
MVD - 125 °C Alumina + 125 °C FGA

C vs. A

- $C = 0.762 \pm 0.001 \ \mu F/cm^2$
- $R^2 = 1.000$
- $d \approx 8.9 \ \text{nm}$
- $\kappa \approx 7.7 \pm 0.02$

$I_{\text{Leak}}$ vs. $V_{\text{DC}}$

- $I_{\text{Leak}} < \text{nA}$
- $V_{\text{BD}} > 3.0 \ \text{V}$
- $E_{\text{crit}} \sim 0.34 \ \text{V/nm}$
MVD - 100 °C Hafnia + 100 °C FGA

**C vs. A**

- $C = 1.33(4) \pm 0.004$
- $1.30(7) \pm 0.003 \ \mu F/cm^2$
- $R^2 = 1.000, 1.000$
- $d = 11.3 \ \text{nm}$
- $\kappa = 17.03 \pm 0.0(5), 16.6(9) \pm 0.03$

**$I_{Leak} vs. V_{DC}$**

- $I_{Leak} < nA$
- $V_{BD} > 5.5 \ \text{V}$
- $E_{crit} \sim 0.49 \ \text{V/nm}$
First PDMS Thickness Experiments

- Si wafer – 500 rpm for 30 s
  - $\mu = 0.75 \text{ mm}, \sigma = 0.06 \text{ mm}$
- Si wafer – 500 rpm for 15 s
  - $\mu = 0.79 \text{ mm}, \sigma = 0.02 \text{ mm}$
- Si wafer – 100 rpm for 15 s
  - Could not accurately measure
- Pyrex dish – let sit
  - $\mu = 3.67 \text{ mm}, \sigma = 0.52 \text{ mm}$
  - Could not remove from mold
- Fluoroware lid – let sit
  - $\mu = 3.46 \text{ mm}, \sigma = 0.16 \text{ mm}$
PDMS Thermal Integrity

- Five squares approximately 10x10 mm² were cut and heated.

- Height and width were measured with calipers at 30 and 60 minutes of heating for various temperatures.

- PDMS was fine up through an hour at 300 °C.
PDMS Thermal Integrity

- Data points → average area ratio
- Error bars → one standard deviation
- PDMS also able to withstand 300 °C H₂/Ar anneal for 1 hour