Appendix

Standard Operating Procedures

A. Fabrication of an oxide hard mask for etching silicon

a. Grow oxide mask using PlasmaTherm CCP-DEP PECVD system for oxide on silicon at 350 °C standard recipe for the amount of time corresponding your your desired oxide mask thickness. To grow 2 μm of oxide on silicon, we approximately 30 minutes.
b. Measure oxide mask thickness using the Nanospec2 (silicon on oxide)
c. Put wafer with oxide mask into YES prime oven for 20 minutes following the standard protocol to coat with HMDS (hexamethyldisilazane) for better photoresist adhesion.
d. Using the SVGcoat to spin and soft bake SPR3612 photoresist @1.6μm. This will be patterned and serve as a mask for patterning the oxide layer.
e. Load the desired mask file into the Heidelberg and after running a test exposure, pattern your wafer.
f. Use the SVGdev to develop and hardbake the photoresist.
g. Descum the wafer with the Technics plasma asher to prepare the surface for oxide wet etching.
h. Isotropic wet etch the wafer with 6:1 BOE (34% Ammonium fluoride (NH_4F), Hydrofluoric acid 7%, 59% water) to pattern the oxide, using photoresist as a mask for 22 minutes, followed by 3 DI water rinses.
i. Strip the photoresist with Piranha (70% - 90% sulfuric acid (H_2SO_4), hydrogen peroxide(H_2O_2) for 10 minutes @ 120 °C, followed by 6 DI water rinses.
j. The wafer now has a silicon oxide mask and is ready for dry etching using the PT-DSE

B. Two step etching with single mask using PT-DSE

a. For etching silicon using the PT-DSE, create or adapt a new recipe that includes at least the following main steps will be 1: Gas stabilization, 2: Light, 3: Etch, 4: Pump Detach. An example of reflected power error is below.
    i. If the etch is pseudo-isotropic, the ICP Match Tune Setpoint Position will need to changed to a setpoint of around 72.0. If the etch is anisotropic and requiring cycling, the setpoint is likely around 65.0.
    ii. In either case, test the recipe for a few seconds on a dummy wafer. First, put the tool in maintenance mode, and click to transfer the material

manually from the load lock to the chamber. Then, place the tool back into production mode and monitor the ICP reflected power to ensure that the value is low (< 50W) before deciding on your setpoint. If the reflected power is too high, stop and abort, change the ICP Match Tune Setpoint and process the recipe again.

iii. ICP Match Tune Setpoint can change for a variety of reasons, including the cleanliness of the chamber, parameters of your recipe and the manner in which they interact with other conditions.

b. Parameters that can be changed:

i. Etch time: change the pseudo-isotropic etch time, holding all variables constant. Loop time: change the number of loops, holding all other variables constant

ii. Bias Voltage: Change the Bias RF Forward Voltage, holding other values constant.

iii. Electrode Temperature: Create and save new recipe steps that change the electrode temperature in every step. Manually transfer the material to the load lock and wait until the electrode setpoint temperature has been reached. Failure to do so will result in reflected/delivered ICP power errors.

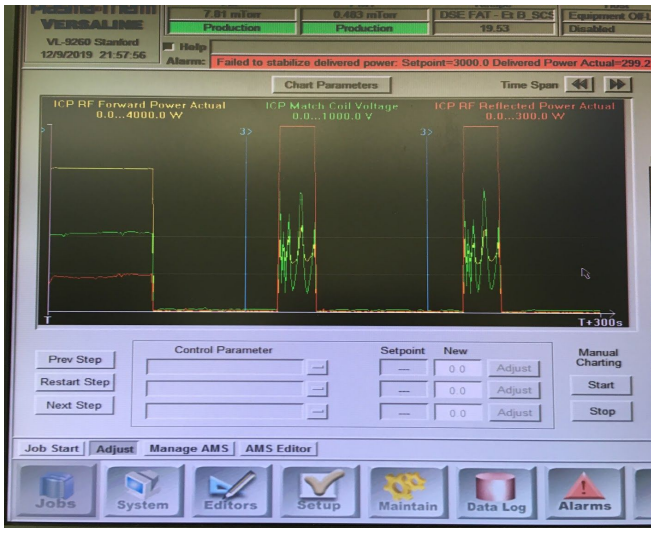
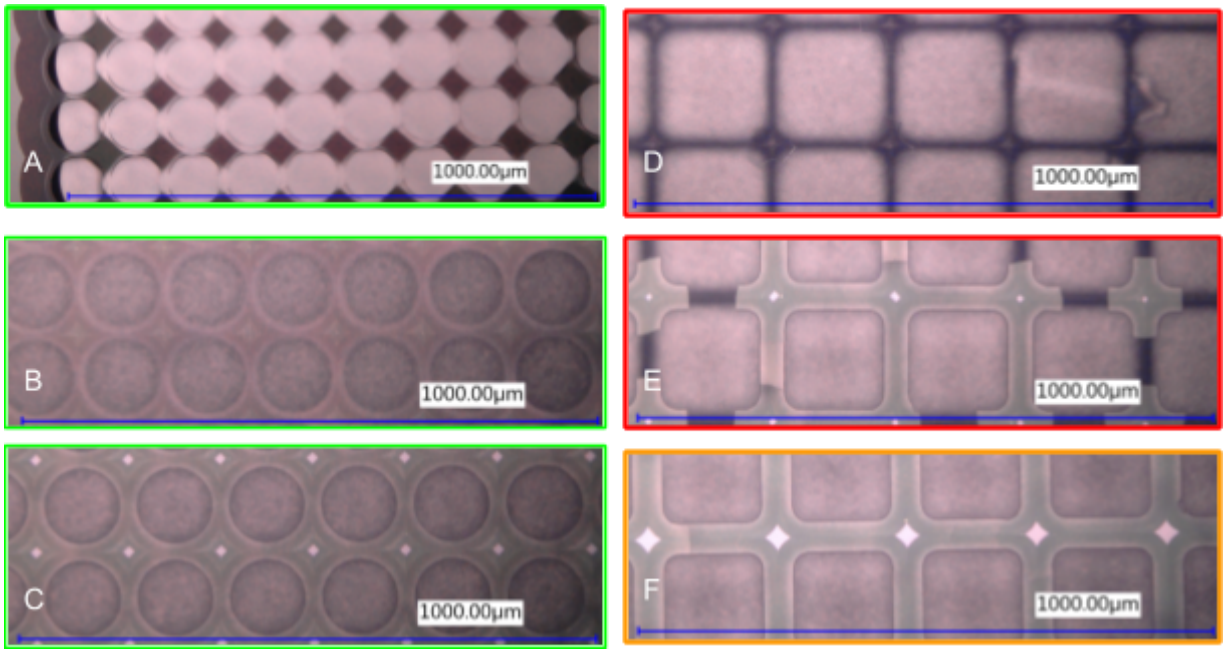


Figure 9. *Example of failure to stabilize delivered and reflected power. Issues with ICP Power mayl arise as demonstrated in this picture.*

Oxide mask insights



Square oxide mask (D-F) tends to crack/flake once the mask is undercut significantly from etching. This problem did not occur with circular mask openings (A-C) and the mask even remained intact after all supporting substrate was etched (A). This is likely due to stress concentrations in the corners of the square mask. This is an important insight for future mask design when we want to etch under silicon oxide. Using a thicker oxide mask, adding a larger radius whenever possible, or reducing the amount of undercut beneath the mask should prevent this from happening.