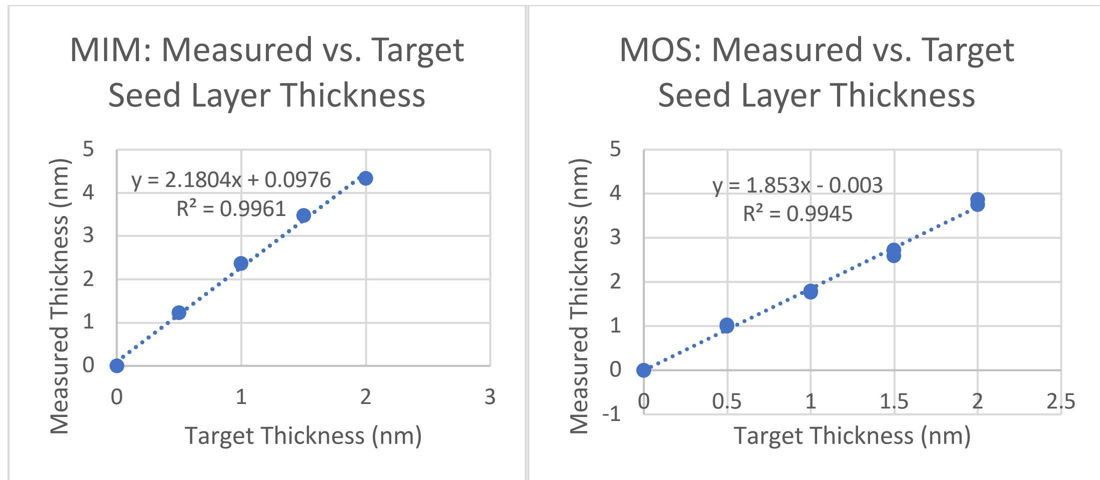
3. SOP

Seeded MOSCAPs and MIM structures on Si substrates: Process and Measurement

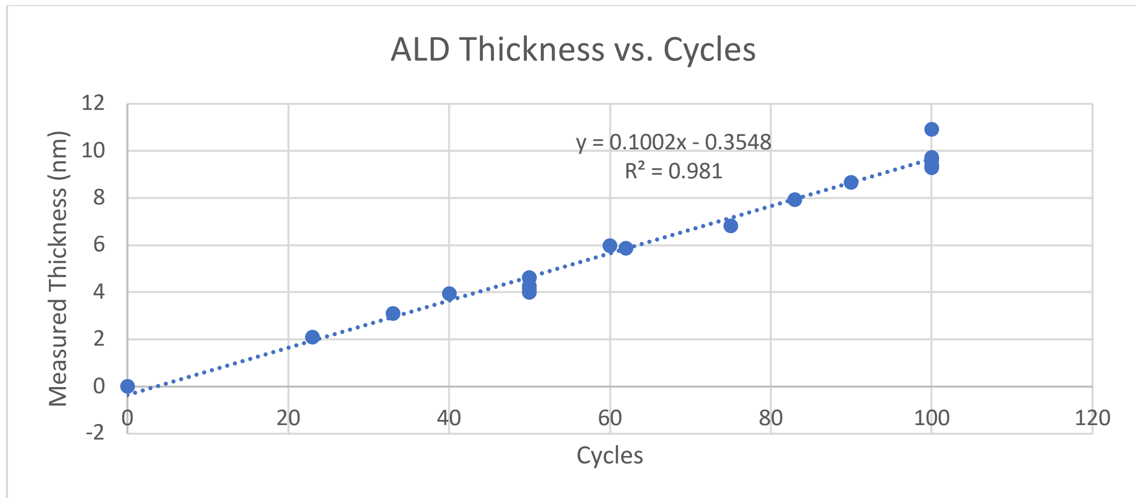
1. Obtain substrate and determine whether final structure will be MOSCAP or pseudo-MIM
    a. The substrate doping and wafer resistivity have a large impact on the electrical characteristics of the final product. The substrate doping will affect whether a p-MOSCAP, n-MOSCAP, or pseudo-MIM structure is formed.
    b. Using a lightly p-type doped substrate will result in a p-MOSCAP being formed, using a lightly n-type doped substrate will result in an n-MOSCAP being formed, and using a heavily-doped substrate will result in a near-metallic low-resistance bottom contact for the MIM structures that will be developed.
    c. In this report, we will show results for p-MOSCAPs (i-test) and highly n-doped pseudo-MIM structures.
2. Perform a standard RCA clean of the wafer
3. (Optional) Cleave the wafer to process different pieces with separate seed layer/ALD thicknesses
4. Measure native oxide thickness with Woollam
    a. This will allow us to later subtract out the native oxide thickness when doing ellipsometry measurements on the seed/ALD layers.
    b. Use the default Woollam measurement settings given on the Woollam wiki page.
    c. In VASE, use Si 1mm, NTVE_OX (fit, guessing 15A).
    d. Ensure that the MSE < 5 and the NTVE_OX fit returns between 5A and 25A.
    e. If the thickness is way off, there may be a thin film already deposited on your substrate.
    f. If the fit is not great, try fitting the n and k parameters, and refitting.
5. Use AJA to deposit seed layer
    a. Blow the surface of the samples with N_2 gun which is at the side of AJA to remove dust.
    b. Load the wafer/pieces into AJA using the correct sample holder.
    c. For alumina, use the Al_0.2A/s recipe which is in the AJA recipe list to deposit the desired seed layer thickness.
        i. Change the target thickness
        ii. This recipe is developed for thin Al film deposition, so for thin seed layer deposition, use this recipe.
    d. Remove the wafer/pieces from the system. With Al deposition, the seed layer should immediately oxidize in the ambient atmosphere (up to 2nm should fully oxidize within an hour based on published results[1] and lab member's findings).
6. Measure seed layer thickness with Woollam
    a. Use Si, NTVE_OX (with the previously measured thickness), use dielectr/Alumina (fit, guess seed layer thickness)
    b. As described in step 4, we can tune dielectr/Alumina layer fit by fitting n and k if necessary.

[1] https://www.spiedigitallibrary.org/conference-proceedings-of-spie/11116/111160O/Using-ellipsometry-and-x-ray-photoelectron-spectroscopy-for-real-time/10.1117/12.2529893.short

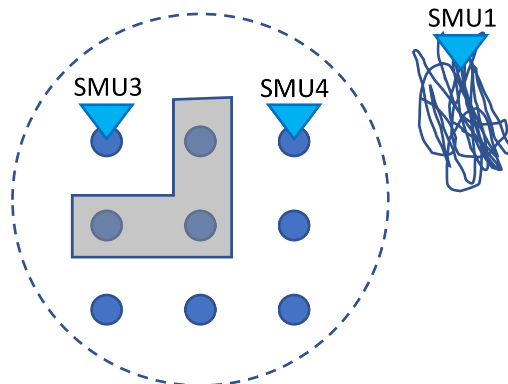
c. Seed layer oxidation is expected to produce larger thicknesses than the seed layer that was deposited. We believe this is due to a combination of oxidative expansion and a poorer oxide quality (lower density).
d. The plot for the ellipsometry measurements of alumina thickness vs. seed layer thickness is given below for the heavily n-doped pseudo-MIM and the p-doped MOSCAP:



7. Use Fiji1/2 to deposit oxide film
    a. Alumina with standard thermal alumina recipe (~1A/cyc)
        i. Thermal Al2O3 STANDARD @ 200C default
    b. Depending on whether you need fine-grained control over your total oxide thickness, you may either:
        i. Subtract your measured seed layer thickness from your total desired oxide thickness to determine the number of cycles to run. We used this approach for our MOSCAPs.
        ii. Ignore the seed layer and run ALD for the desired number of cycles. This is useful for running multiple samples at once when testing multiple seed layer thicknesses. We used this approach for our MIM structures.
8. Measure final oxide thickness with Woollam
    a. Use Si, NTVE_OX (with the previously measured thickness), dielectr/Alumina (fit, guess measured seed layer thickness + expected ALD thickness)
    b. Tune n,k if needed
    c. ALD thickness fit is given below:



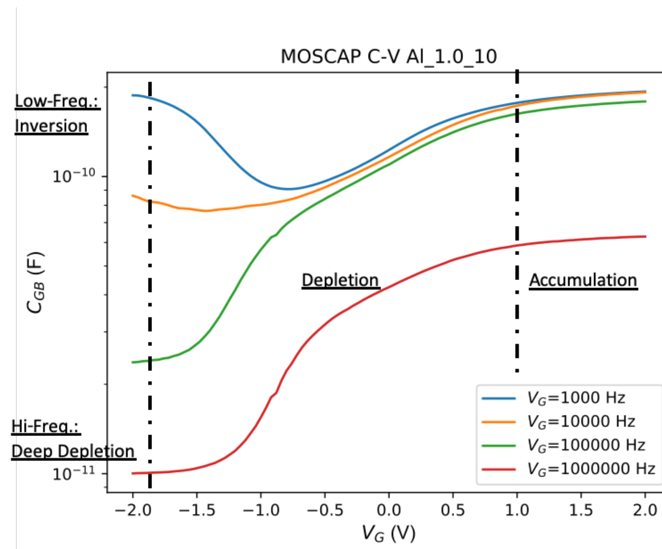
9. Obtain shadow mask and prepare samples for patterned deposition
    a. Obtain a shadow mask that contains holes for defining the top contacts of the MIM structures you wish to measure. We used a shadow mask with 200-micron diameter holes. It is possible to put multiple samples under the shadow mask if the samples are small enough and the mask is large enough.
    b. Run Ti 0.5A/s recipe for a final thickness of 5 nm. This layer is for adhesion since Au is not very hard or good at sticking to other materials.
        i. Ti_0.5A/s recipe
    c. Run Au 1A/s recipe for a final thickness of 20 nm.
        i. Au_1A/s recipe
10. Fabrication complete! Now begin measurements with micromanipulator6000.
11. Open micromanipulator6000 and load the akashl_E241 workspace.
12. Scratch surface of sample
    a. The scratches dig under the oxide layer and enable one of your probes to contact the substrate directly.
    b. Scratch oriented away from your contacts to minimize dust getting on contacts.
13. Contact SMU1 probe to scratched area
14. Identify a 3x3 grid of contacts that have no dust



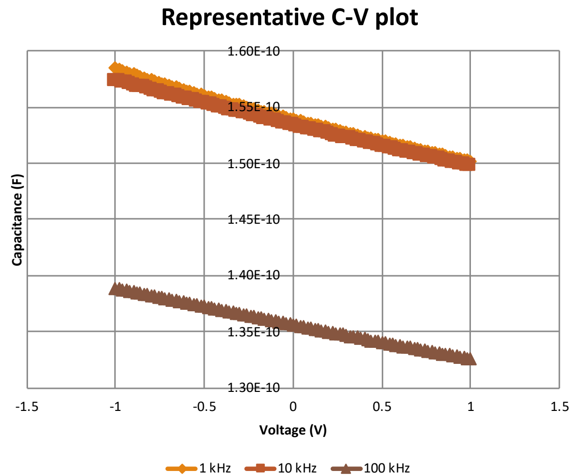
15. Contact SMU3 probe in top-left corner contact
16. Breakdown top-left corner structure

a. Use Backgate Breakdown test
   i. Bidirectional 0V – 50V sweep (101 steps each way) on SMU3
   ii. 50 mA compliance current
   iii. SMU1 grounded, SMU4 floated
b. Advantage: now backgate contact is physically closer to structures being tested
c. Less IR-drop through substrate (less wafer resistance when contacts are closer)
d. You should see a low current that jumps up very quickly to a high current beyond a certain threshold voltage. See the I-V curves below to understand what dielectric breakdown looks like.

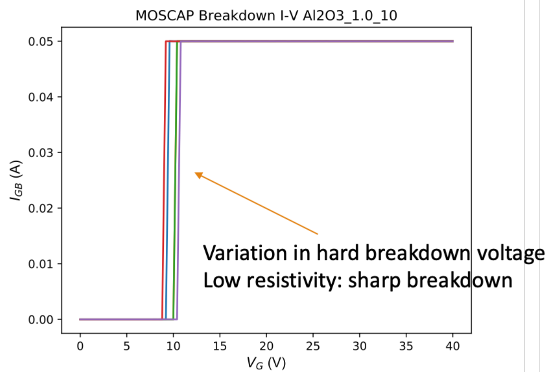
17. Contact SMU4 to 3 closest contacts for C-V
   a. See gray area in figure above
   b. Use C-V Sweep formula
      i. Bidirectional -1V – 1V sweep (101 steps each way), measuring Rs-Cs b/w SMU3 and SMU4, no delay, 50 mA AC signal
      ii. 1kHz, 10kHz, 100kHz, 1MHz, 5MHz measured C-V frequencies
      iii. SMU1 floated
   c. For MOSCAP, you should see MOS behavior
      i. At low frequency, you should see inversion, depletion, and accumulation regions
      ii. At high frequency, you should see deep depletion, depletion, and accumulation regions
      iii. An example is given below

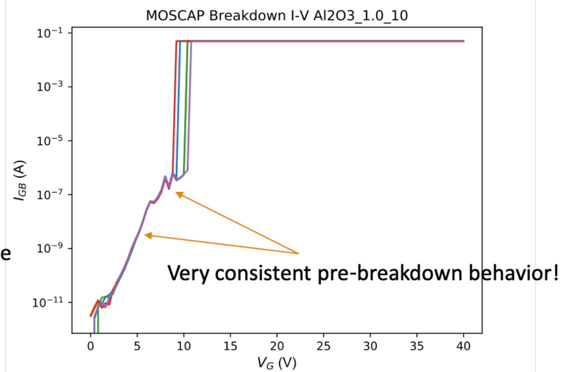


   d. For MIM structures, you should see nearly constant capacitance as shown below

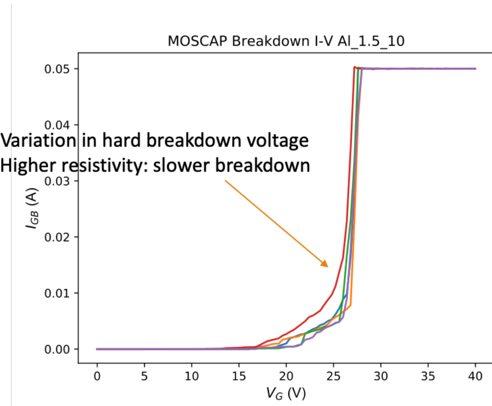


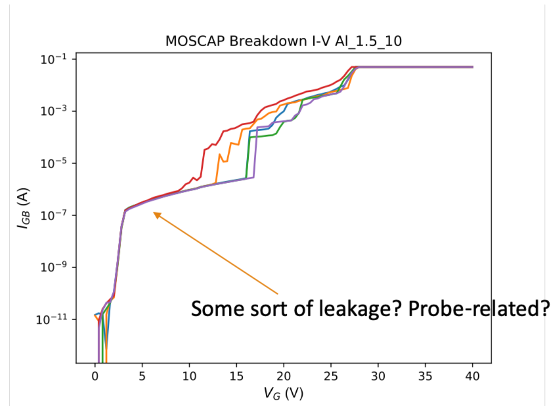
18. Contact SMU4 to 5 remaining outer contacts for breakdown measurements (I-V)
    a. Use Breakdown formula
        i. Unidirectional 0V – 50V sweep (101 steps) on SMU4
        ii. 50 mA compliance current
        iii. SMU1/SMU4 grounded
    b. For MIM structures, you should see sharp breakdown behavior where the current is near zero and shoots up to the compliance current at some threshold voltage





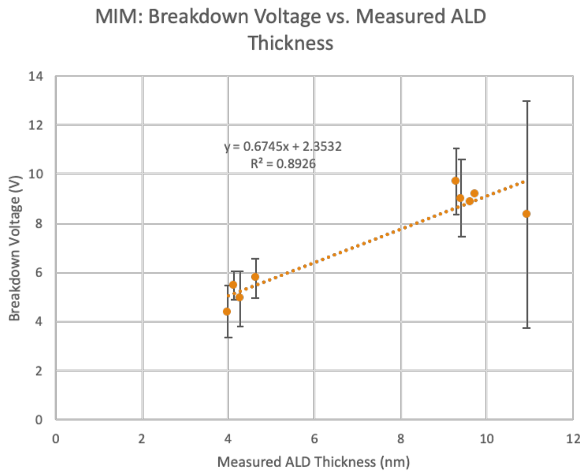
    c. For MOS structures, you may see less sharp breakdown behavior depending on the resistivity of the substrate and the exact doping profile

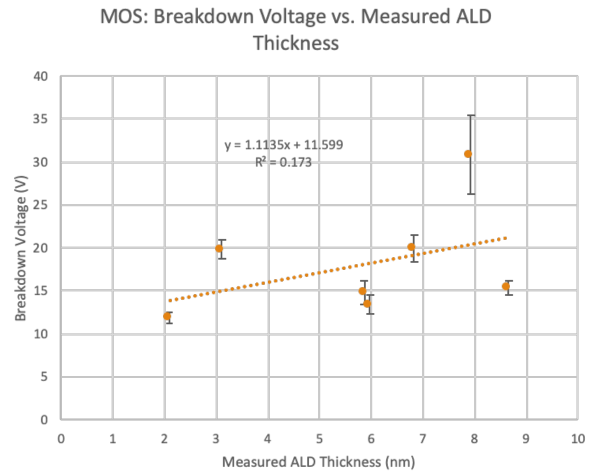




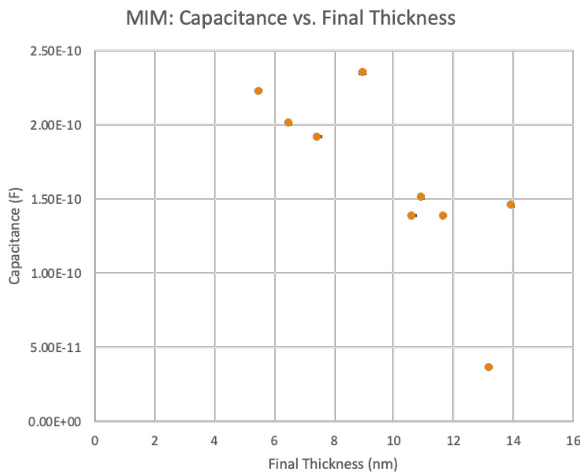
d. In either case, you can expect to see variation in the breakdown threshold voltage due to intrinsic variations in the breakdown behavior device-to-device

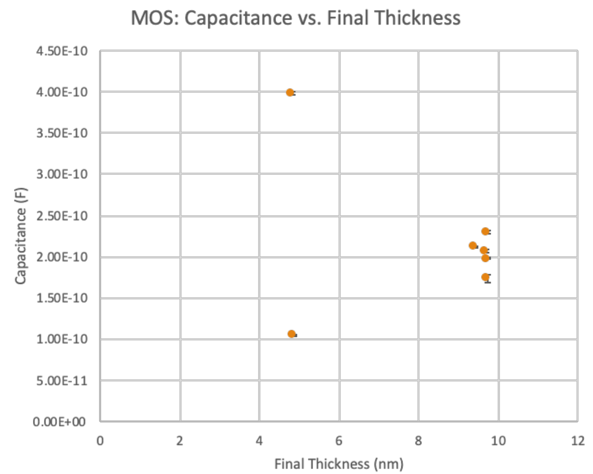
19. Compute desired values



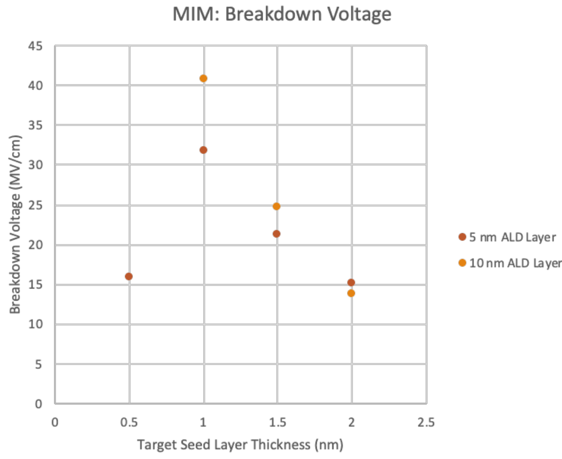


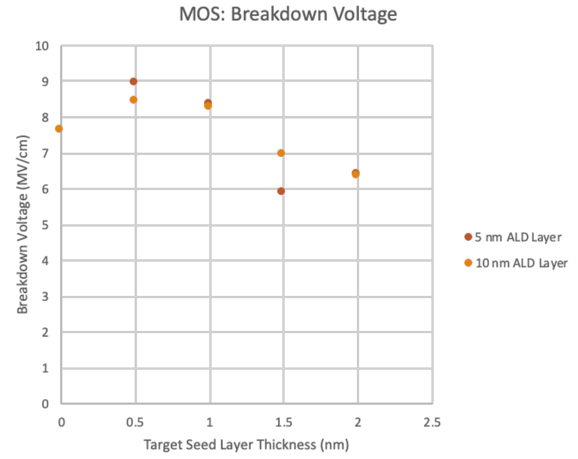
Breakdown voltage is defined as 1st intersection of I-V curve with 1mA current threshold





Capacitance is extracted from low-frequency (1kHz) C-V curve @ 1V





Note: # of ALD cycles was NOT dependent on seed thickness here

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