SOP Descriptions

Part A - Fabricating hollow pillar chip for high throughput electrophysiological measurements & Making large amounts of nanostructures of various shapes using photolithography & two-stage etching processes

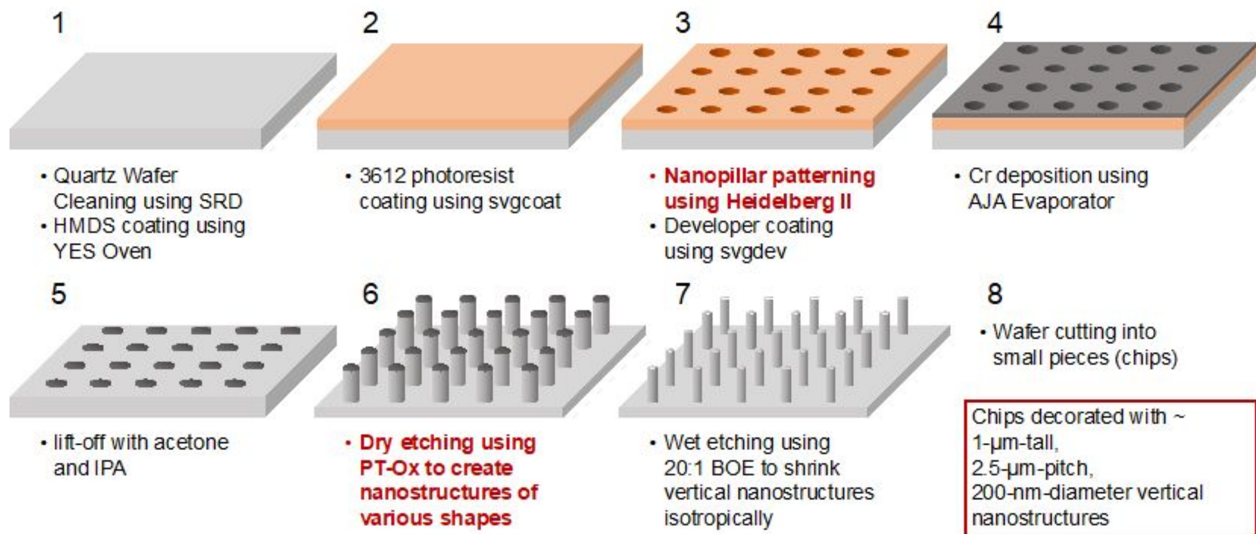

Figure 1. Schematic illustration of the fabrication procedure for making vertical nanostructures with different shapes on the quartz surface.

1. Wafer Cleaning and Nanostructure Patterning

1-1. Rinse wafers using SRD
- Apply the recipe 1 to wash (default recipe).

1-2. Coat clean wafers with HMDS (HexaMethylDiSilazane) using YES oven
- Apply the recipe 1 to bake (default recipe).

1-3. Coat HMDS-covered wafers with photoresist using svgcoat (automatic track)
- Select the program which applies “3612 1µm w/o vp 2mm EBR” photoresist to wafers.

1-4. Exposure photoresist-coated wafers with desired patterns using Heidelberg2
- Substrate Template: Wafer 4 inch (Round shape)
- Layer: Only monolayer exposure (FirstExposure only)

- Parameters:
  - Designed pattern: NegCurvDesign_ChingTing
  - Design Size: 81.8 x 81.4 mm
  - Design Type: Binary
  - Laser wavelength: 375 nm
  - Laser dose: 132 mJ/cm^2
  - Defoc: -2
- Select “Expose with substrate angle” and “Auto-Unload the Substrate”.

1-5. Bake and Develop patterned wafers using svgdev

- First-run - Developer program #9 (null) + Oven program #1 (Baking only)
- Second-run - Developer program #3 + Oven program #1 (Developing + Baking)

1-6. Check the patterns on the wafers under the microscope

2. Nanostructure Fabrication

2-1. Deposit Cr on patterned wafers using AJA evaporator

- Parameters:
  - Rate: 1Å/s
  - Thickness: 120 nm (1.2kÅ)

2-2. Lift off immediately at wetflexsolv (solvent bench)

- Rinse wafers with acetone for 2 min (avoid acetone evaporation!), then sonicate wafers in acetone for 5 min.
- Rinse wafers with isopropyl alcohol (IPA) for 2 min, then sonicate wafers in IPA for 5 min.
- Gently dry wafers with nitrogen gas.

2-3. Dry etching using PT-Ox

- Before start:
  - Check the badger and enable the tool. If the tool is disabled, “facilities service has failed” alarm will pop up on the plasma-therm control screen.
  - Check the transfer arm has been set to the correct wafer size configuration.
  - On the plasma-therm screen, make sure there are no active alarms on the system. Process state is in “Stand-by” mode.
- Use the dummy wafer to clean the chamber:
  - Choose the “Ws_O2 Clean” recipe to run the cleaning process. Click “Go to recipe temperature”. check AL and PM1 are both in the production mode.Vent the loadlock.
  - Load the dummy wafer. Align the flat bottom with the line marked on the arm, then close the load lock.

- Make sure the recipe sequence and recipe steps are correct and have the desired settings.
- Select “Vent after Job”, then click “Start Job”.
- Click “Jobs”/”Adjust” to monitor the process. Monitor ICP forward, ICP reflected, temperature and pressure.

- Etch sample wafers:
  - After the cleaning is done, put the dummy wafer on top of the sensor on the right-hand side of the load arm, and load the sample wafer. Align the flat bottom with the line marked on the arm, then close the load lock.
  - Make sure the recipe sequence and recipe steps are correct and have the desired settings.
  - Select “Vent after Job”, then click “Start Job”.
  - Since quartz wafers are transparent, the sensor is unable to detect the wafer. It’s necessary to ‘trick’ PT-Ox in order to sense the wafer and proceed the etching process. To do so, First click “maintain” button. Choose “AL” and change its status into “Maintenance” mode. Click “Edit material” and delete wafer detected in the loadlock. Go back to the AL chamber status and switch its mode back to the “Production” mode.
  - Select the program “XiaoLi_Ox_C4F8”. The RIE condition used is listed below:
    - C_4F_8 flow rate (sccm): 80
    - H_2 flow rate (sccm): 40
    - Ar flow rate (sccm): 20
    - Bias Power (W): 200
    - ICP Power (W): 1500
    - Pressure (mT): 7
    - Etching time （change it at the step 3 “Process Time Setpoint”): 180-540 sec (180 sec leads to ~1-μm-tall vertical nanostructure; 360 sec causes ~2-μm-tall one; 540 sec causes ~3-μm-tall one. Please mind that the length of etching time is dependent on the shape, density of the pattern and substrate type.)

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- ○ After the process is done, take out the sample wafer and the dummy wafer.
- ○ Pump down the loadlock and disable the tool.

2-4. Wet etching at wetflexcorr (corrosive solution bench)

- Incubate dry-etched wafers in Cr etchant for 15-20 min to remove the Cr mask.
- Incubate the wafers in 20:1 BOE for 5-10 min to shrink vertical nanostructures isotropically.
- Wash the wafers with ddH_2O. Gently air flows to remove liquid on the wafers.

2-5. Hollow electrodes fabrication (Optional)

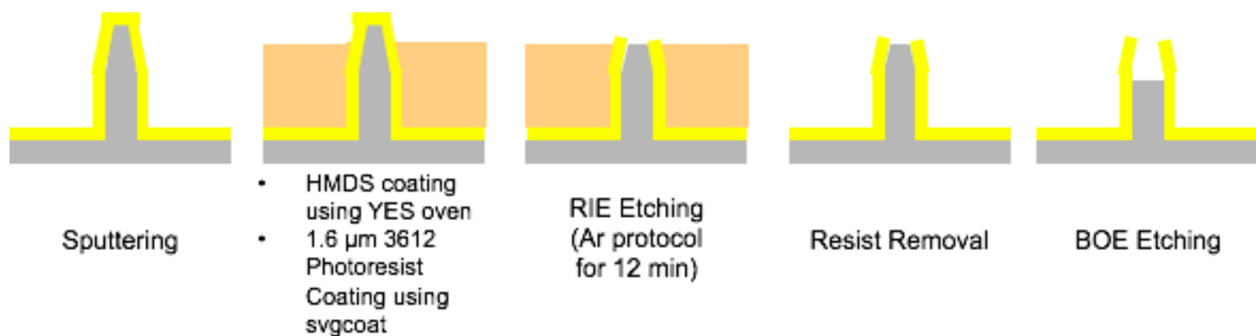

Figure 2. Schematic illustration of the fabrication procedure for creating hollow pillars on quartz surface.

- Select nanoelectrodes with defined shape
- Deposit Ti at 5nm/min for 120 s (10nm) using Lesker Sputter
- Deposit Pt at 10nm/min for 240s (40nm) using Lesker Sputter
- Put in YES oven default cycle at SNF (20 min)
- Coat with Shipley 3612 1.6 um w/o vp 2mm EBR
- Dry etch using mrc tool for 12 min (Ar = 15 sccm, Chamber Pressure = 12.5 mT, RF Power = 100 W, Peak Voltage = 660 V) to remove the metal coating on top
- BOE for 6 min to etch through the center of the electrode

2-6. Cut patterned wafers into small pieces for the biological applications