

Low-T, High- κ Dielectrics for Transparent and Flexible 2-Dimensional Electronics

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Abstract

Interest in transparent and flexible electronics and their possible applications has increased greatly in the last few years, and several research groups spanning multiple departments at Stanford have joined in. However, transparent/flexible substrates such as PDMS and PEN typically demand very strict thermal budgets, while most standard high- κ ALD processes require deposition temperatures of 200 °C or higher. Herein, we have investigated the electrical quality of oxides deposited in both the Savannah and MVD ALD systems at deposition temperatures down to 100 °C and examined the compatibility of PDMS and PEN substrates with standard optical lithography techniques. All oxides are characterized by fitting thicknesses via ellipsometry and measuring the capacitance, dielectric constant, breakdown voltage, and C-V hysteresis of MIM capacitor arrays.

Introduction

Novel materials for use in transparent and flexible electronics have picked up increased interest recently [1], and many research groups at Stanford have begun investigating these materials for niche applications. Polydimethylsiloxane (PDMS) and polyethylene naphthalate (PEN), being cheap, lightweight, and non-toxic, show promise as both transparent and flexible substrates for other materials, especially 2D materials such as graphene and transition metal dichalcogenides (TMDs). With the new capabilities for processing PDMS available in ExFab at Stanford, SNF users can now begin to investigate the viability of this material for such applications. However, PDMS and PEN are only rated to be operational up to 200 and 155 °C, respectively [2,3], and most standard high-k atomic layer deposition (ALD) processes require deposition temperatures of at least 200 °C, if not higher. Additionally, ALD oxides to be used for gates often require post-deposition annealing at even higher temperatures. Therefore it is necessary to develop low temperature ALD recipes that are compatible with transparent and flexible substrates.

Herein we have investigated the quality of both alumina and hafnia oxides deposited by ALD in the Savannah and MVD systems in the Stanford Nanofabrication Facility (SNF). Oxide variables included deposition temperature, annealing gas, and annealing temperature. The electrical quality of these oxides was quantified with capacitor arrays by measuring capacitance, dielectric constant, breakdown voltage, and C-V skew. Additionally, we attempted to fabricate similar capacitor arrays on PDMS and PEN in hopes of elucidating processing issues that might be unique to these materials, and subsequently narrowed the processing window for which these substrates remain viable, though no capacitors have been successfully fabricated to date.

Part I – Oxide Benchmarking

The design of experiments (DoE) began by reviewing previous work that had been documented for the ALD processes available in SNF. Only one report was found that studied alumina and hafnia film quality as a function of deposition temperature [4], but these Savannah-deposited films were only evaluated by measuring thickness, leakage current, and breakdown voltage. Because we are mainly interested in utilizing these oxides as gates for metal-oxide-semiconductor field-effect transistors (MOSFETs), we planned our DoE to reevaluate these oxides for their values of normalized capacitance and dielectric constant, in addition to film thickness, C-V skew, leakage current, and breakdown voltage; we also decided that all ALD recipes would consist of 100 cycles of pulsed precursor and deionized H₂O (DI), since it is well-known within the SNF community that this number of cycles yields pinhole-free oxides; and finally, we resolved to briefly analyze the differences between post-ALD annealing in forming gas and oxygen ambients.

Methodology

The fabricated structures were arrays of metal-insulator-metal (MIM) capacitors with areas ranging from 100 to 10,000 μm^2 . C-V measurements were performed first, from which we extracted values for skew and capacitance. By using capacitors of varying sizes, we were subsequently able to fit a line to a plot of capacitance vs. area, from which we extracted both the intrinsic normalized capacitance of the oxide as well as any parasitic capacitance that might be associated with the pads. Using thickness values obtained via ellipsometry and a two-plate capacitor model, we then calculated a dielectric constant for the oxide. Finally, quick a DC voltage sweep up to 10 V was performed to evaluate both leakage current and breakdown characteristics. Further details for processing, measurement, and analysis are given below.

Standard Process Flow

A brief cartoon of our process flow is shown in Fig. 1 along with fabrication details. The details of lithography, metallization, liftoff, and O_2 treatment were the same for all structures fabricated.

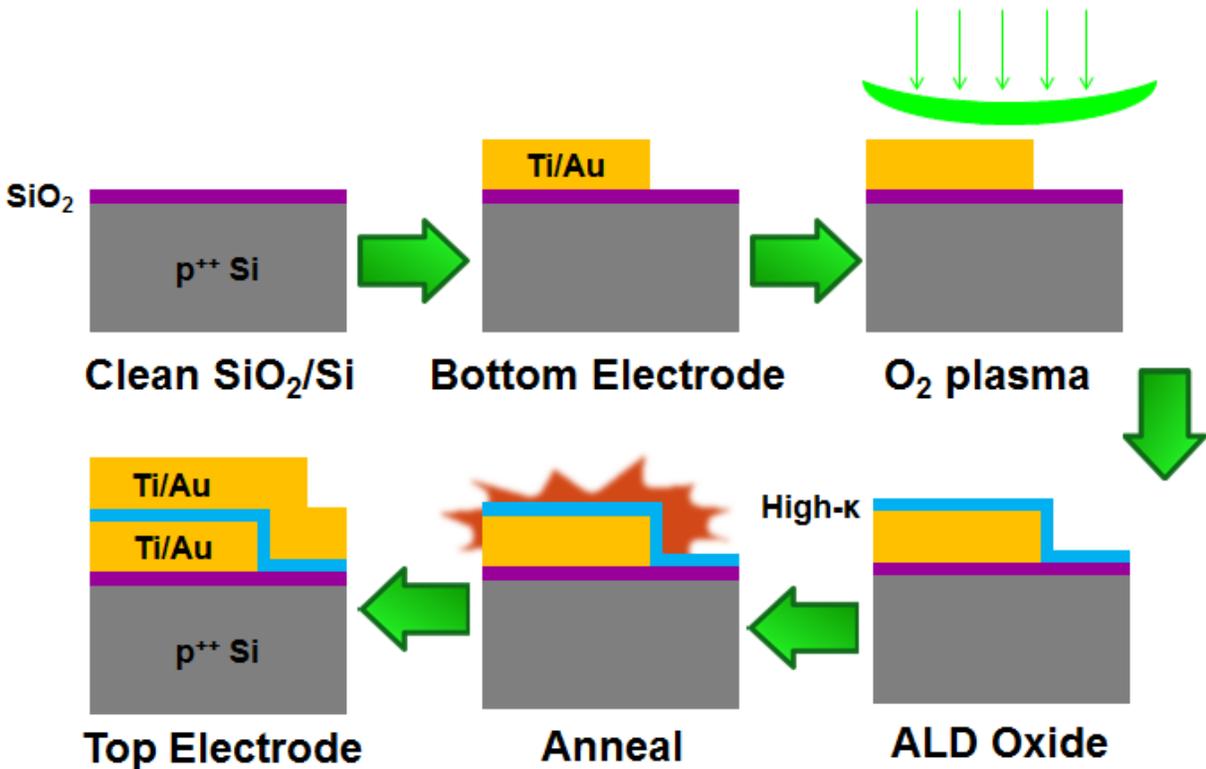


Fig. 1: Cartoon schematic of typical process flow, showing bottom electrode metallization, O_2 plasma treatment, ALD oxide deposition, annealing, and top electrode metallization.

All capacitors were fabricated on wafer pieces of thermally grown SiO_2/Si (p^{++}). The thickness of the SiO_2 was 7 nm for the Savannah oxides and 285 nm for the MVD oxides; the 7 nm SiO_2/Si (p^{++}) stack

ends up contributing significant parasitic pad capacitance that is common to all MIM caps on those chips, but this term is easily removed by our extraction technique, discussed below.

Lithography began by spinning on a liftoff resist (LOR), PMGI SF6, at 3000 rpm for 60 seconds using Headway2. LOR for the Savannah oxides was baked at 200 °C for 5 minutes, whereas LOR for the MVD oxides was baked at 150 °C for 10 minutes to verify that the LOR still functions as intended with a reduced thermal budget. (Although this will alter the undercut rate during development [5], our structures were large enough that no discernible difference was observed during liftoff.) SPR 3612 was subsequently spun on at 5000 rpm for 40 seconds and baked on a hotplate at 90 °C for 60 seconds.

Exposure was done with the KarlSuss contact aligner using the 365 nm I-line, hard-contact mode with a 40 µm gap, for 1.2 s. Post-exposure baking was done on a hotplate at 115 °C for 60 seconds, after which the chips were developed in MF-26A for 45 seconds before being thoroughly rinsed with DI.

Metallization was performed in a Kurt J. Lesker PVD 75 electron beam evaporation chamber. All electrodes consisted of 2 nm Ti followed by 38 nm Au. Liftoff was achieved by allowing the chips to soak in Remover PG at room temperature for at least two hours before being sprayed with acetone.

Following bottom electrode definition, the ALD chamber was preconditioned with the same film to be deposited for 100 cycles. Immediately before loading into the ALD chamber, the chips were treated with O₂ plasma using the MRC reactive ion etcher for 120 seconds (20 sccm O₂, 20 mTorr, 50 W) to both remove resist residue and make the substrate hydrophilic. After depositing 100 cycles of the intended recipe by alternating pulses of DI and trimethylaluminum (TMA) or tetrakis(dimethylamido)hafnium (TDMA-Hf), the chips underwent forming gas annealing in the gold contaminated AllWin for 15 minutes. (All Savannah oxides were annealed at a temperature 50 °C above deposition temperature, whereas MVD oxides were annealed at the same temperature as deposition, again to reduce thermal budget. One set of chips underwent oxygen annealing, but the oxide quality was not found to deviate significantly from those annealed in forming gas.) Oxide thicknesses were fit to ellipsometry data taken on blank dummy wafer pieces (with no fabricated structures) with the Woollam.

Finally, following another round of lithography, metallization, and liftoff, finished MIM capacitor arrays were measured as detailed below. Typical recipes for alumina and hafnia oxides can be found in Appendix I.

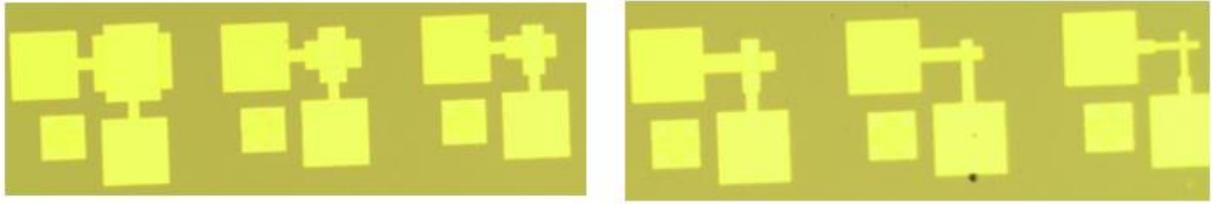


Fig. 2: Optical microscopy images of completed capacitor arrays. Electrodes overlap in squares with sides of 10, 20, 30, 40, 50, and 100 μm .

Measurement Setup

All electrical measurements were performed in air, at room temperature, using a Janis probe station and Keithley 4200 Semiconductor Characterization System. C-V measurements were taken by sweeping the DC bias from 0 to 1 to -1 to 0 V while superimposing a 30 mV 100 kHz ac signal between two probes, while two additional probes measured the phase shift, from which capacitance is automatically calculated using a parallel admittance model. It should be noted that open- and short-configuration compensation was performed for the cables and probes to account for parasitic impedances of the instrumentation, and identical C-V curves could be produced using a series admittance model.

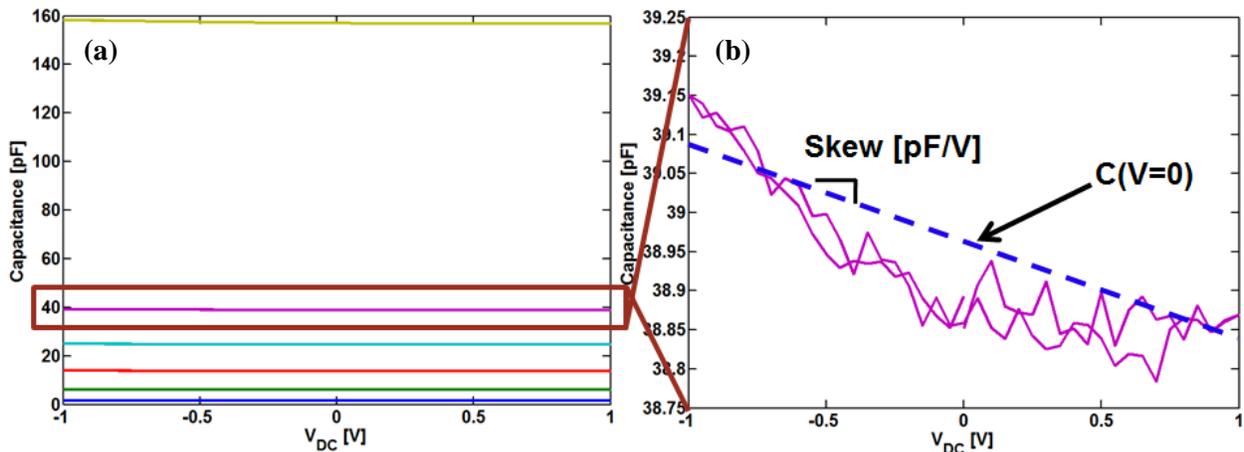


Fig. 3: (a) Capacitance vs. DC voltage measurements for six hafnia capacitors in an array. (b) Zoomed-in view of data for the $50 \times 50 \mu\text{m}$ capacitor in (a) along with a linear fit.

For all chips, at least two arrays of capacitors on separate die were measured to help gauge film consistency. Because each array has six capacitors, C-V sweeps such as that shown in Fig. 3a were produced. A zoomed in view of one of these C-V measurements showing noise is shown in Fig. 3b; in order to systematically extract values from these somewhat noisy sweeps, a line was fit to each C-V measurement. The fit slope of this line is reported below as “skew” [pF/V], and the ordinate intercept of

the fit was value used for further analysis. It should be noted that since the capacitance values of these MIM structures change by less than 1% over the range of C-V measurements, the extracted values of normalized oxide capacitance and dielectric constants reported herein also vary by less than 1% if the analysis is done using the fit values at ± 1 V.

Parameter Extraction and Analysis

Plotted in Figs. 4 – 6 are a representative sample of capacitance vs. area and leakage current vs. DC bias plots. Data for two arrays of capacitors are plotted in all cases, demonstrating the consistency of oxide quality across at least cm scales. Data and fits for all other ALD films can be found in Appendix II.

Concerning the plots of C vs. A, it can be seen for the Savannah oxides that the linear fits have an ordinate intercept very close to 4 pF for both the alumina and hafnia films, indicating that this parasitic capacitance is common to both sets of capacitors. Furthermore, the MVD oxides show an ordinate intercept fit very close to 0 pF, indicating very low parasitic capacitance. Because this parasitic capacitance is common to all Savannah oxides regardless of type, deposition temperature, and annealing temperature, and this parasitic capacitance is not seen for MVD oxides, which were fabricated on much thicker SiO₂, we concluded that this parasitic capacitance arises from the thin 7 nm SiO₂/Si p⁺⁺ stack common to all Savannah chips.

It should be noted that if one were to calculate a dielectric constant for each individual capacitor, six different values would be obtained due to this parasitic contribution, and the errors would be especially large for the smaller area capacitors. However, the advantage of our methodology allows us to remove this parasitic contribution via the linear fit, the slope of which produces a more uniform estimate of C/A that is only intrinsic to the ALD oxide. We can then estimate the dielectric constant by using a parallel plate capacitor model:

$$\frac{C}{A} = \frac{\kappa\epsilon_0}{d} \quad \text{Eq. 1}$$

The alumina and hafnia films also exhibit very different breakdown behaviors. Below 3 V, both alumina and hafnia showed a linear increase in leakage current with DC bias; the observations that this leakage is the same for all oxides and capacitor sizes indicates that this is either filamentary conduction or perhaps related to the noise floor of the instrumentation. Past ~3 V however, all alumina films experienced what appeared to be a soft breakdown, as the current increased exponentially until a hard breakdown closer to 7 or 8 V. The hafnia films, on the other hand, exhibited a purely linear I-V relationship up to 4 or 5 V, at which point a hard breakdown destroyed the capacitors.

Savannah: 150 °C Al₂O₃ + 200 °C FGA

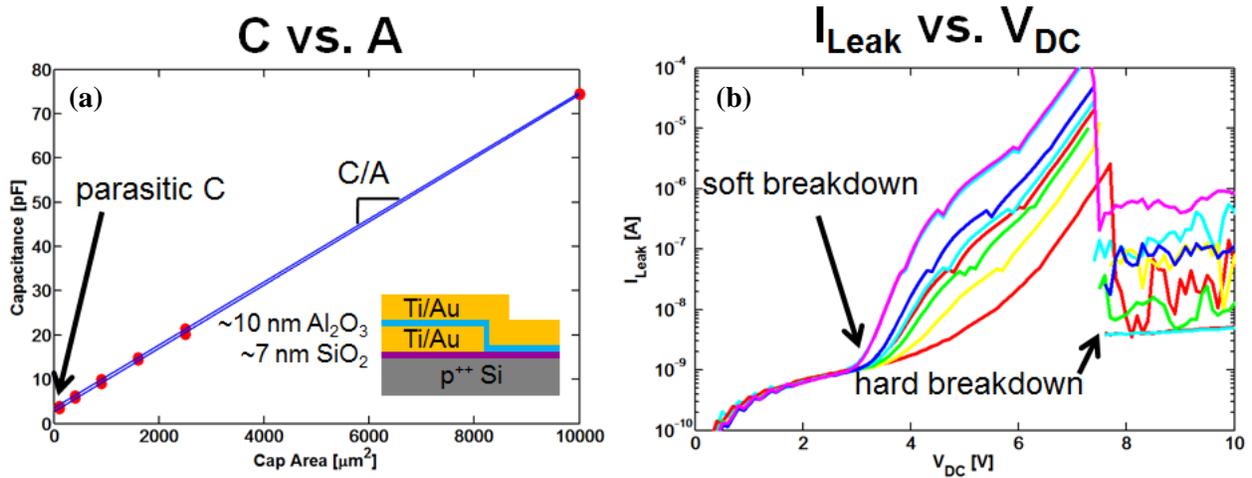


Fig. 4: Data for Savannah alumina deposited at 150 °C and annealed in forming gas at 200 °C. (a) Capacitance vs. area and linear fits, showing a parasitic contribution from the thin SiO_2/Si (p^{++}) substrate. (b) Leakage current vs. DC bias of the same capacitors in (a), exhibiting both soft and hard breakdown thresholds.

Savannah: 150 °C HfO₂ + 200 °C FGA

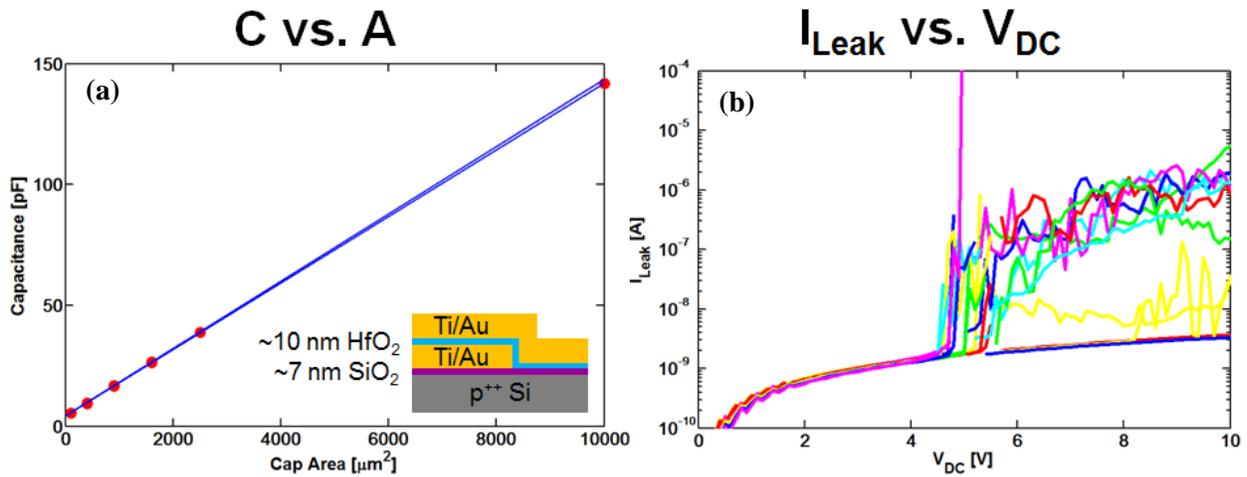


Fig. 5: Data for Savannah hafnia deposited at 150 °C and annealed in forming gas at 200 °C. (a) Capacitance vs. area and linear fits. (b) Leakage current vs. DC bias of the same capacitors in (a), exhibiting only a hard breakdown threshold.

MVD: 125 °C Al₂O₃ + 125 °C FGA

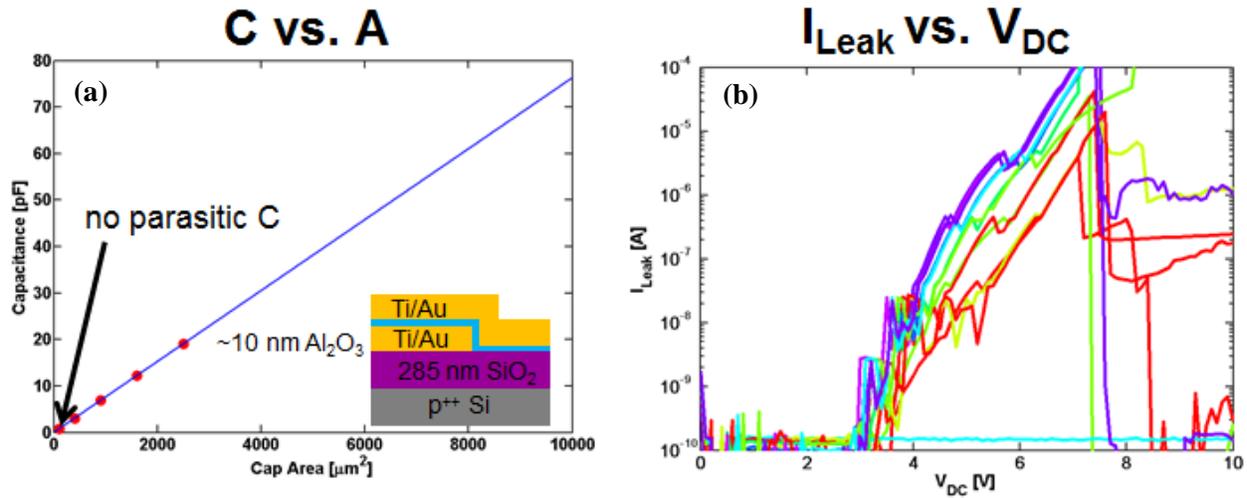


Fig. 6: Data for MVD alumina deposited at 125 °C and annealed in forming gas at 125 °C. (a) Capacitance vs. area and linear fits, showing no parasitic contribution from the 285 nm SiO₂/Si (p⁺⁺) substrate. (b) Leakage current vs. DC bias of the same capacitors in (a).

Results

Tabulated below are the compiled data for the ALD oxides investigated, detailing ALD deposition temperature, annealing conditions, oxide thickness, skew, normalized capacitance, dielectric constant, leakage current, breakdown voltage, and critical electric field.

Savannah Oxides

Savannah	Alumina				Hafnia			
ALD temp	200 °C	200 °C	150 °C	100 °C	200 °C	200 °C	150 °C	100 °C
anneal	+ 50 °C O ₂	+ 50 °C FGA			+ 50 °C O ₂	+ 50 °C FGA		
d [nm]	10.0	10.0	9.4	8.4	8.7	8.7	10.5	11.9
Skew [pF/V]	~-0.15	~-0.01	~-0.15	X	~-0.2	~-0.2	~-0.1	~-0.15
C [$\mu\text{F}/\text{cm}^2$]	0.670	0.690	0.715	X	1.51	1.61	1.39	1.15
κ	7.6	7.8	7.6	X	14.8	15.8	16.4	15.5
I _{Leak}	<nA	<nA	<nA	X	<nA	<nA	<nA	<nA
V _{BD} [V]	>3.5	>3.5	>3.0	X	>3.2	>3.2	>4.5	>6.0
E _{crit} [V/nm]	0.35	0.35	0.32	X	0.37	0.37	0.43	0.50

Table 1: Results for Savannah oxides deposited between 100 and 200 °C, showing physical and electrical data.

MVD Oxides

MVD	Alumina		Hafnia	
	125 °C	100 °C	125 °C	100 °C
ALD temp	125 °C	100 °C	125 °C	100 °C
FGA	125 °C	100 °C	125 °C	100 °C
d [nm]	~8.9*	6.9	~11.2*	11.3
Skew [pF/V]	~-0.05	X	~-0.7	~-0.4
C [$\mu\text{F}/\text{cm}^2$]	0.760	X	1.57	1.32
κ	~7.7*	X	~16*	13.2
I_{Leak}	<nA	X	<nA	<nA
V_{BD} [V]	>3.0	X	>5.5	>5.5
E_{crit} [V/nm]	~0.34	X	~0.49	0.49

*d interpolated from Savannah data

Table 2: Results for MVD oxides deposited at 100 and 125 °C, showing physical and electrical data. Thicknesses for 125 °C oxides were not fit with the Woollam, and so thickness values have been estimated by interpolating from Savannah data.

Although the Savannah and MVD films are very similar in terms of capacitances, dielectric constants, leakage, breakdown, and overall trends, there are notable difference between the alumina and hafnia films. Other than the fact that the hafnia films yield substantially higher capacitances than alumina of comparable thicknesses, the two exhibit opposite trends as a function of temperature. As deposition temperature decreases, the alumina films became thinner, whereas the hafnia films grew thicker. Consequently, the capacitance of the alumina films increased while that of the hafnia decreased; yet because of the inverse relationship between oxide thickness and capacitance, the dielectric constants remained nearly constant (to within 10%) across the observed temperature range. This also caused the breakdown voltage for low temperature alumina films to decrease and that for hafnia to increase.

Furthermore, no capacitor arrays fabricated with the 100 °C alumina in either the Savannah or MVD could be measured. Although these capacitors did show low leakage values consistent with the higher temperature oxides, only nonsensical and inconsistent values for capacitance could be obtained during C-V sweeps, and so we determined that the alumina ALD process is not stable at 100 °C. Hafnia, on the other hand, appears to be a perfectly stable and uniform process as low as 100 °C.

Concerning post-ALD annealing treatment of the 200 °C oxides, although forming gas seems to yield slightly higher values for capacitance and dielectric constant, the difference is too small to draw any definitive conclusions that one gas is better than the other for annealing. Forming gas was chosen for annealing all subsequent samples.

Overall, the ALD alumina and hafnia films seem to be consistent between the Savannah and MVD, and across a range of temperatures down to 125 °C. 100 cycles of either process yields films in the neighborhood of 10 nm (~1 Å per cycle), and the leakage remains below the nA level for DC biases up to several volts, though the alumina films exhibit an exponential increase in current at a bias significantly lower than the breakdown threshold for hafnia. Finally, the extracted dielectric constants tend to be near 7.7 for alumina and 16 for hafnia, allowing for capacitances in excess of 1 $\mu\text{F}/\text{cm}^2$ to be easily achieved.

Part II – Transparent/Flexible Substrates

After benchmarking the quality of oxides on SiO_2 substrates, we next moved to fabricate the same capacitor array structures on PDMS, a flexible and transparent material recently added to the nanostructures integration lab (nSiL), as well as PEN. The original intent of this portion of the study was to examine how resilient these oxides are after experiencing tensile and/or compressive strain. However, after several iterations of failed fabrication experiments and extensive troubleshooting, it was determined that the PDMS and standard PEN substrates were unsuitable for photolithography, as detailed below. Nevertheless, we were able to accumulate a wealth of processing knowledge, should future researchers ever endeavor to utilize PDMS or PEN as a substrate for lithography. A summary table of standard processing techniques comparing PDMS and PEN to SiO_2/Si is provided below.

	Hotplate Curing	Ovens $\geq 150\text{ }^\circ\text{C}$	Direct SPR 3612	Oxide/Metal Cracking	Thermal Wrinkling	Trivial Alignment
SiO_2/Si	yes ✓	yes ✓	yes ✓	no ✓	no ✓	yes ✓
PDMS	no ✗	no ✗	no ✗	yes ✗	yes ✗	yes ✓
PEN	yes ✓	no ✗	? ?	no ✓	no ✓	no ✗

Table 3: Summary table of standard processing techniques and issues showing compatibility or lack thereof for SiO_2/Si , PDMS, and PEN substrates.

Processing Dos and Don'ts for PDMS

PDMS processing began by mixing and curing PDMS “wafers” as described in Appendix III. After cutting 1.5×1.5 cm squares out of the wafer using a razor blade, the PDMS pieces were placed on bare 2×2 cm Si wafer pieces that had been thoroughly cleaned with acetone, methanol, and isopropanol (but not O_2 plasma, which tends to cause a more permanent adhesion). The inherent stickiness of the PDMS was enough for adhesion during photoresist spinning and alignment while still allowing itself to be manually removed later. The final pre-lithography step was to cap the PDMS pieces with Scotch tape, to both cover

the sticky PDMS surface as well as remove any particles that had adhered to the surface in the moment before.

The first lithography attempt mimicked that of standard processing for SiO₂/Si pieces, and the outcome is shown in Fig. 7. In short, LOR was spun on at 3000 rpm and baked on a hotplate at 200 °C for 5 minutes, after which visible wrinkles could be seen along the edges of the PDMS square, but not in the center. Because it was assumed the few mm of PDMS would provide too high a thermal resistance for baking optical resist on a hotplate in only 60 seconds, SPR 3612 was subsequently spun on at 5000 rpm and baked in the 90 °C oven for 25 minutes. After standard exposure with the KarlSuss and development in MF-26A (which posed no additional problems due to the Si support wafer), metallization and liftoff were performed as detailed in the “Standard Process Flow” section above. We quickly noticed that the wrinkles caused by the thermal stresses on the hotplate caused resist to be non-uniformly exposed, leading to metal remaining between features near the edges; bubbles were also seen to exist under pads near the center of the chip.

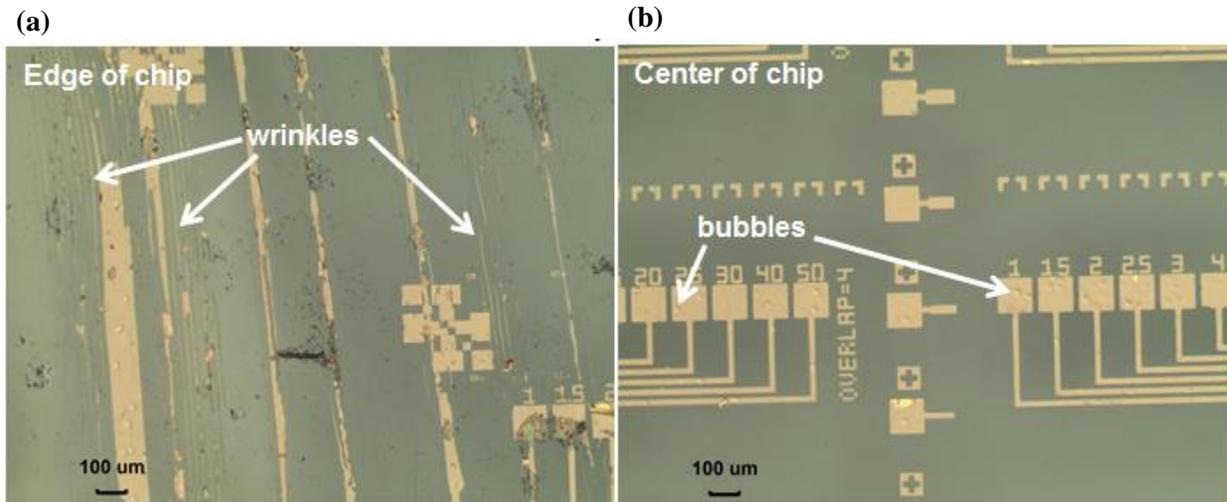


Fig. 7: First PDMS processing iteration, after resist spinning, baking, exposure, development, metallization, and liftoff. (a) Optical image of the edge of the chip, showing wrinkles. (b) Optical image of the center of the chip, showing bubbles.

In an effort to resolve these nonidealities, several more tests were done to explore the compatibility between standard resist processing and PDMS in SNF. The only change for the second iteration was to bake the LOR in the white oven at 230 °C instead of on a hotplate, to reduce possible thermal gradients that may have caused wrinkling. But as illustrated in Fig. 8, this caused wrinkles on all areas of the PDMS, likely owing to the largely increased thermal budget in the oven. The third iteration, the results of

which are shown in Fig. 9, again changed the LOR baking step, this time comparing both the white oven and hotplate treatments at 150 °C. Similar to iteration 2, wrinkling was seen across the entire chip.

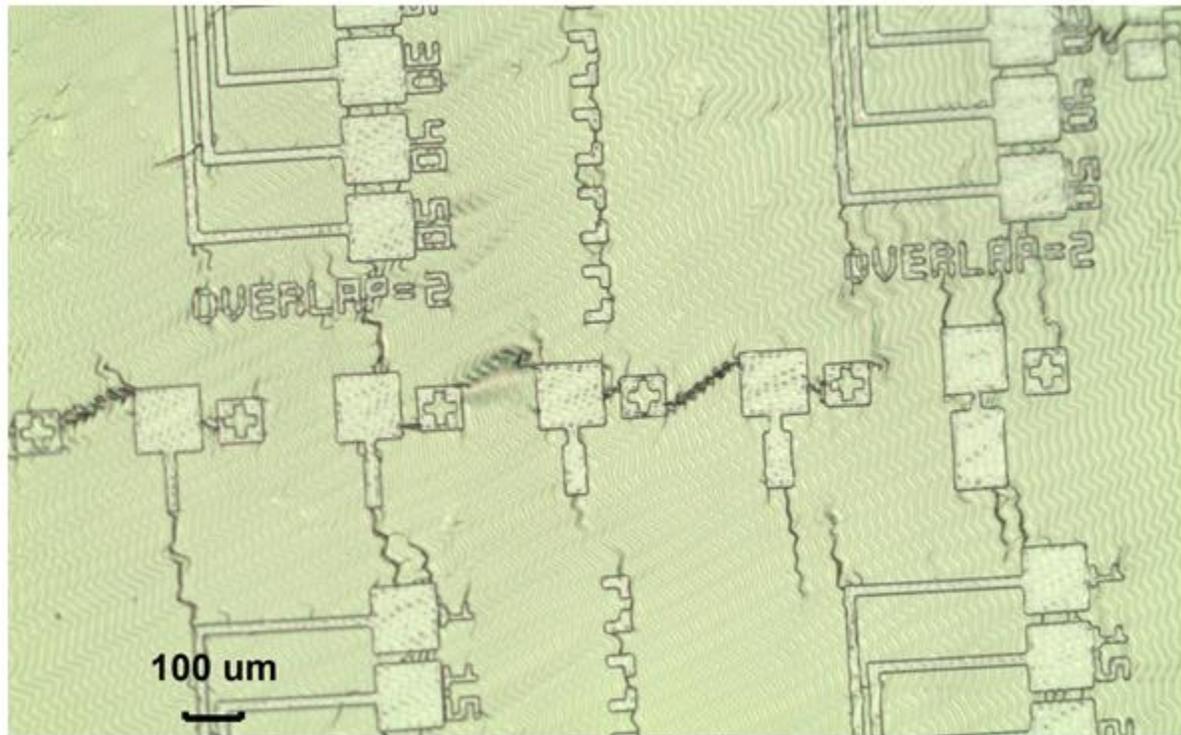


Fig. 8: Second PDMS processing iteration, after resist spinning, baking exposure, and development. Wrinkles propagate over the entire substrate due to the excessive heat and large coefficient of thermal expansion.

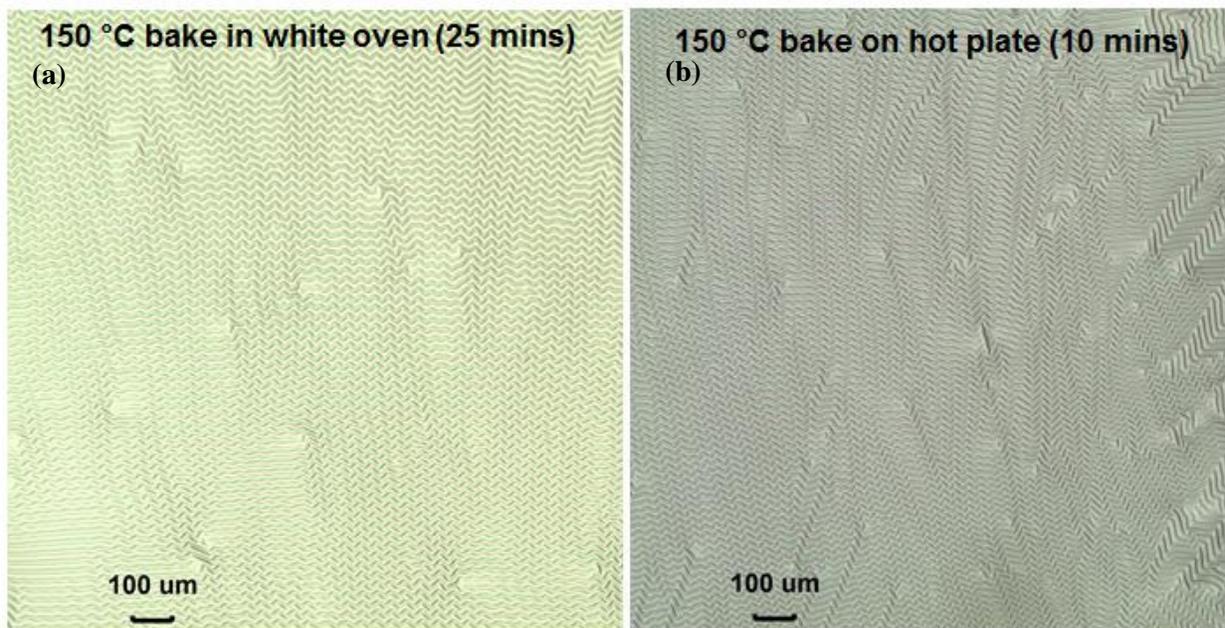


Fig. 9: Third PDMS processing iteration, after resist spinning and baking. (a) and (b) Optical images of the center of each chip, showing wrinkling across the entire substrate regardless of baking method at 150 °C

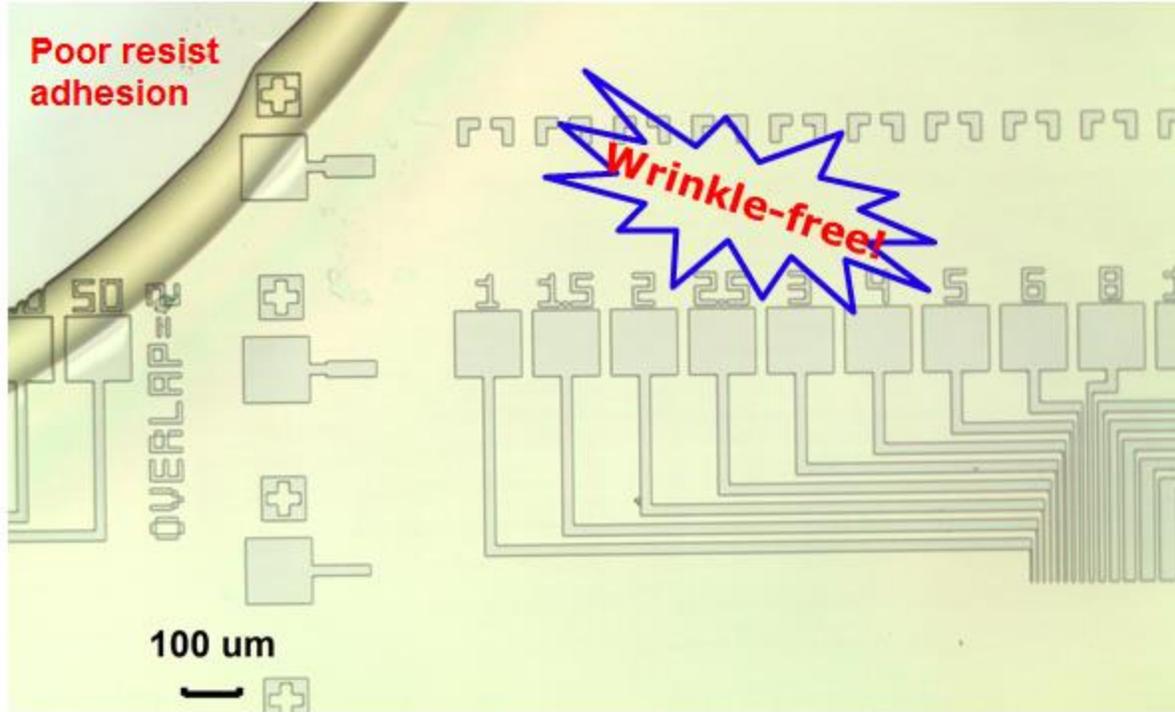


Fig. 10: Fourth PDMS processing iteration, after resist spinning, baking, exposure, and development. Although not using a LOR allows for a lower thermal budget and mitigates the wrinkling issue, there is poor resist adhesion between the SPR 3612 and the PDMS surface.

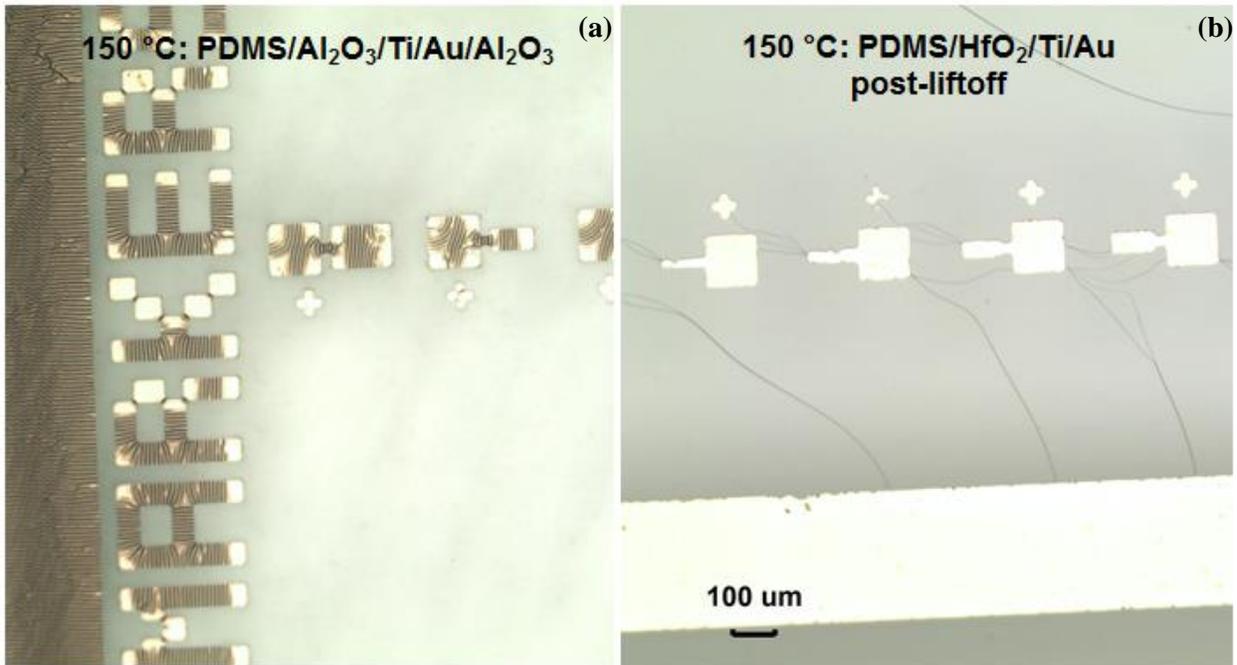


Fig. 11: Sixth PDMS processing iteration, after buffer ALD deposition, resist spinning, baking, exposure, development, metallization, and liftoff. **(a)** Optical image of the alumina sample with the second ALD oxide deposited, intended for MIM capacitors, showing that the ALD oxides can wrinkle just as badly as photoresist. **(b)** Optical image of the hafnia sample, showing cracks that remained after the metallization step and uneven metal features. The same wrinkling and cracking is observed in PDMS with ALD processing as low as 100 °C.

Having determined that this wrinkling was occurring because of the high thermal budget demanded for curing LOR, we next decided to remove this step altogether and only apply SPR 3612 and bake in the 90 °C oven. Fig. 10 shows the mixed results of this trial – there was no wrinkling observed anywhere on the chip, but SPR 3612 adhesion to the PDMS was very poor (less than half of the surface remained covered). We went ahead and evaporated Ti/Au and performed liftoff as before to see if the lack of LOR was detrimental to the liftoff process. For our relatively large features ($\geq 10 \mu\text{m}$), there was little difference in the outcome after liftoff, indicating that the LOR step could be removed completely. This observation also led us to the conclusion that any processing at or above 150 °C was outside the thermal budget for PDMS. Our fifth attempt at PDMS processing involved adding a layer of HMDS in the YES oven to aid with resist adhesion. Although not pictured, there was no discernible difference in resist adhesion between iterations 4 and 5.

Knowing that resist seems to have little problem sticking to thermal SiO_2 even without HMDS, we decided for our sixth iteration to deposit 100 cycles of ALD oxides on the PDMS *before* any lithography processing (O_2 plasma was again used as a pre-ALD treatment as outlined previously, and all ALD for PDMS and PEN was performed in the MVD). SPR 3612 was successfully spun onto this PDMS/high- κ stack, with no wrinkling observed before or after the 90 °C oven bake step. Metallization, liftoff, and ALD were subsequently performed, and two typical outcomes are illustrated in Fig. 11. One common observation was a cracking of the metal film after metallization but before liftoff, which caused metal features to be distorted and for cracks to remain on the substrate. Thermal wrinkling of top oxides was also visible, even at ALD temperatures as low as 100 °C. Despite overcoming the lithography issues, we closed our investigation of PDMS as a transparent/flexible support substrate by concluding that the thermal budget allowed by the large coefficient of thermal expansion was much too small even for non-standard, low-T ALD oxides.

Processing Dos and Don'ts for PEN

Noting that the coefficient of thermal expansion was the bane of PDMS, we began investigating another transparent/flexible material as a possible substrate candidate: PEN. The PEN investigated here was standard 250 μm PEN film purchased from Goodfellow [6]. Fig. 12 shows post-development and post-liftoff optical images of features that have gone through our Standard Process Flow. At first glance (i.e., low magnification), no processing issues were observed. Upon closer inspection, however, black specks hundreds of nm in size could be seen both on and off of the deposited metal (see Fig. 13a). Further inspection of unprocessed PEN revealed similar particles. Extensive cleaning was performed in an attempt to rid the surface of these particles, including room temperature baths of SC1 and SC2 as well as

30 minutes of sonication in acetone. Although none of these worked in removing the particles, it should be noted that PEN is robust to most chemical processing. Despite this, in light of the lithography and metallization going smoothly, we decided to move forward with this off-the-shelf PEN to investigate any further processing issues that could arise.

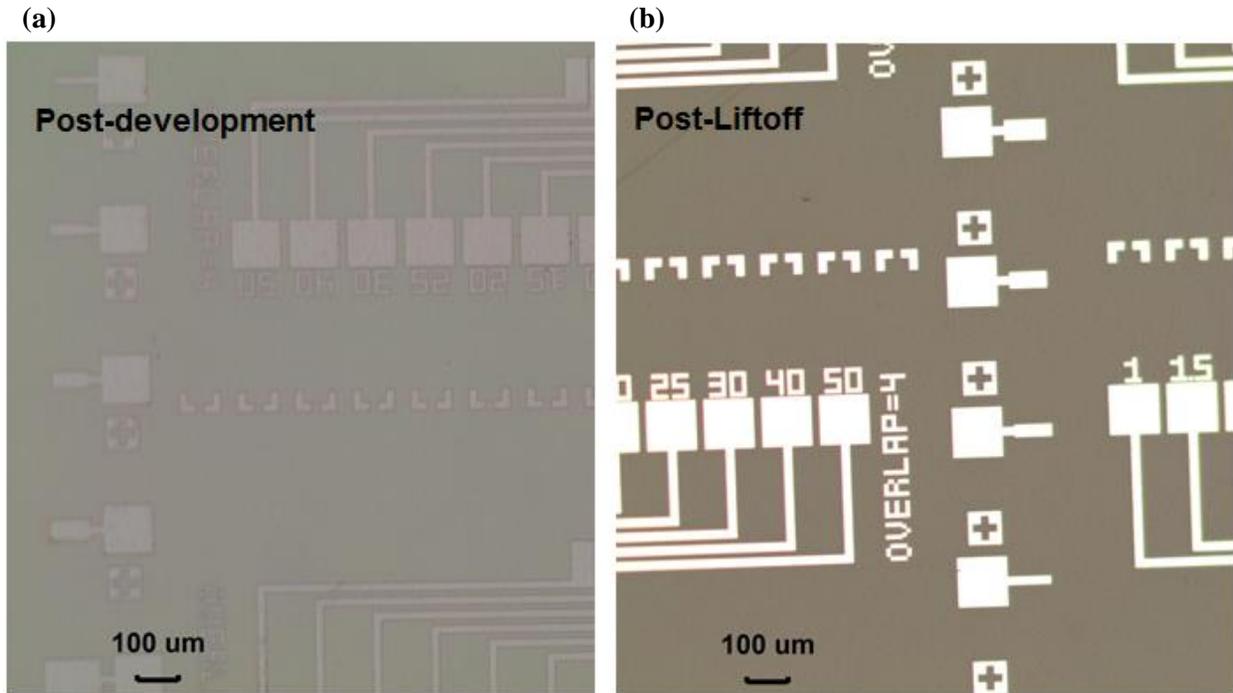


Fig. 12: First PEN processing iteration, after resist spinning, baking, exposure, and development. (a) Optical image showing there are no issues with resist wrinkling even with a LOR. (b) Optical image after metallization and liftoff, again showing no processing issues.

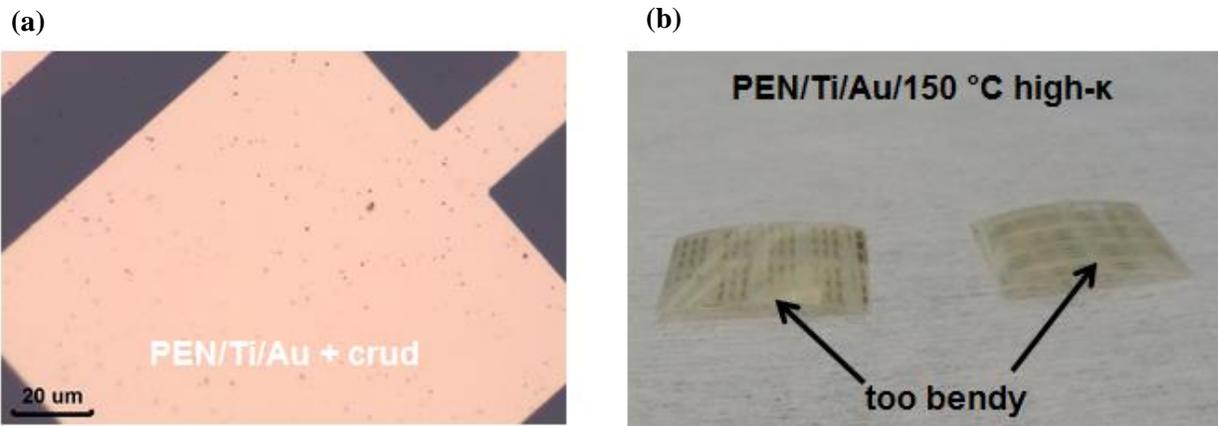


Fig. 13: First PEN processing iteration after metallization and liftoff. (a) Optical image showing numerous black specks that are several hundreds of nm across. (b) Optical image after deposition of the ALD oxide at 150 °C, showing the permanent deformation that high heat can cause in PEN.

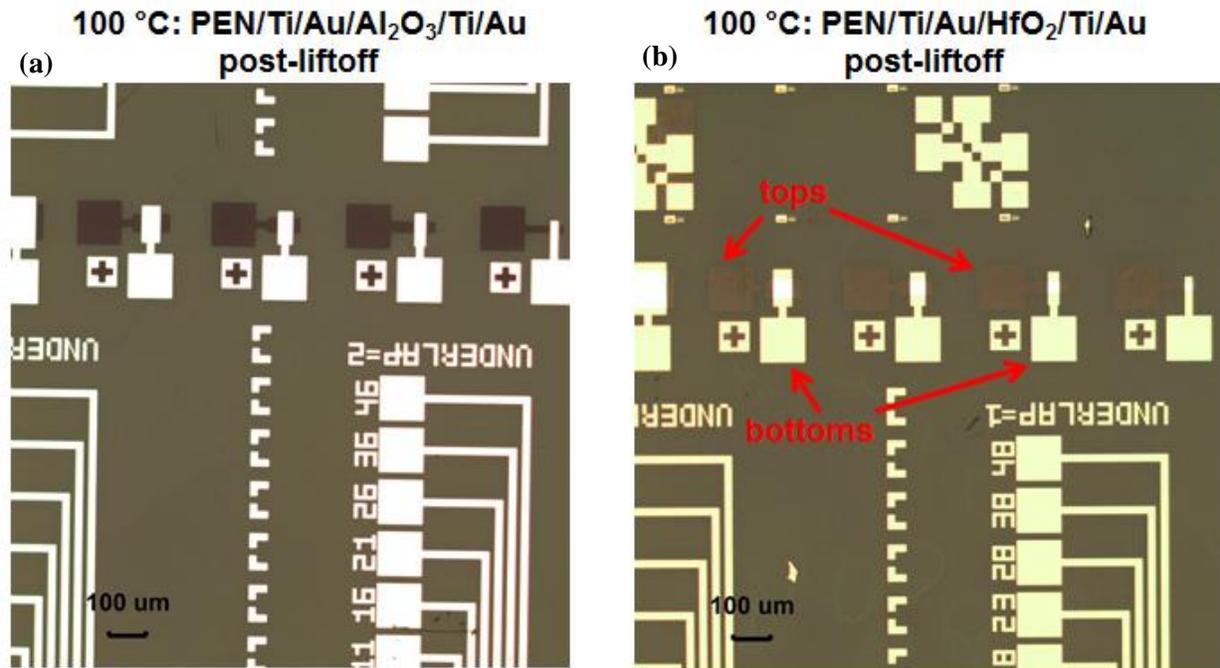


Fig. 14: Second PEN processing iteration, after ALD at 100 °C and a second metallization/liftoff step. **(a) and (b)** Optical images for the alumina and hafnia films, showing failure of the top electrode to fully stick to the oxide. The same thing was observed for PEN with ALD processing done at 125 °C.

Our first attempt at depositing ALD oxides was done in the MVD at 150 °C. Although no wrinkling was observed, the long amount of time spent so close to the published working temperature of PEN (155 °C [6]) caused a permanent bending deformation, shown in Fig. 13b. This bend was stiff enough that the Headway2 could not achieve vacuum for subsequent resist spinning, and also prevented other standard tricks from being used, including using resist or Kapton tape to secure it to a support wafer. Due to this inability of PEN to be processed after deposition of oxides at 150 °C, we determined this temperature to be outside the processing window for PEN as well (though hotplate baking of LOR at 150 and 200 °C did not cause this deformation).

Similar processing was performed with MVD oxides deposited at 100 and 125 °C as well, and no subsequent issues arose in any tools that need to achieve vacuum to operate. Following the second round of lithography, metallization, and liftoff, however, we observed that the top electrode Ti appeared to stick to the oxide, but the Au did not stick to the Ti (see Fig. 14). This sticking issue occurred for both PDMS and PEN on oxides deposited at 100 and 125 °C and for Ti/Au deposited in multiple tools. Whether this problem is rooted in the physical properties of low-T oxides, the flexibility of the substrates, or could perhaps be mitigated with different electrode metals requires further investigation. Notwithstanding this

issue, we attempted to measure the fabricated structures, but could not obtain sensible capacitance measurements. The top contact pads were also found to be considerably more resistive than the bottom, further indicating that the Au did not stick to the Ti.

Nevertheless, we have determined the 125 °C high- κ oxides deposited in the MVD to be within processing windows that allow PEN to remain a workable substrate, and for SNF ALD processes to yield high-capacitance, low-leakage dielectrics. Future efforts will involve obtaining highly transparent, electronics-grade PEN films [7] and continuing to smooth processing issues for structures fabricated with the 125 °C MVD oxides.

Conclusion

In summary, we have investigated the quality of oxides in both the Savannah and MVD ALD tools in SNF and found the two to yield very similar results. For 100 ALD cycles depositing both alumina and hafnia films, the processes were found to produce good-quality, low-leakage oxides down to 125 and 100 °C, respectively. We also attempted to fabricate structures via standard optical photolithography techniques on both PDMS and PEN substrates, and found PDMS to be sub-optimal due to its stickiness, hydrophobicity, and large coefficient of thermal expansion. PEN, however, offers an alternative that is much easier to work with and can tolerate a significantly higher thermal budget. High- κ oxides deposited at 125 °C in the MVD have been identified as prime candidates for developing thin-film transistors out of 2D materials on PEN, and investigation into the intercompatibility of these non-standard materials will be the subject of future work.

References

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- [2] <http://www.dowcorning.com/applications/search/products/Details.aspx?prod=01064291>, accessed 7 Dec 2015.
- [3] https://www.teijinDupontFilms.jp/english/product/pen_teo.html, accessed 7 Dec 2015.
- [4] Y. Wu, S. Yu, and S. Li, *EE412 Fall 10: ALD Oxide Nanolaminates Final Report*, SNF Wiki.
- [5] http://www.microchem.com/Prod-PMGI_LOR.htm, accessed 7 Dec 2015.
- [6] <http://www.goodfellow.com/E/Polyethylene-naphthalate-Film.html>, accessed 9 Dec 2015.
- [7] http://www.teijinDupontFilms.jp/english/product/pen_teo.html, accessed 9 Dec 2015.

Appendix I – Savannah/MVD ALD Recipes

	INSTRUCTION	CHAN	VALUE	UNITS
0	flow	0	20	sccm
1	heater	8	125	°C
2	heater	9	125	°C
3	stabilize		0	sec
4	wait		300	sec
5	pulse TMA	3	0.03	sec
6	wait		15	sec
7	pulse DI H ₂ O	4	0.03	sec
8	wait		15	sec
9	goto	5	100	cycles
10	flow	0	10	sccm

	INSTRUCTION	CHAN	VALUE	UNITS
0	flow	0	20	sccm
1	heater	8	125	°C
2	heater	9	125	°C
3	stabilize		0	sec
4	wait		300	sec
5	pulse TDMA-Hf1		0.3	sec
6	wait		15	sec
7	pulse DI H ₂ O	4	0.03	sec
8	wait		15	sec
9	goto	5	100	cycles
10	flow	0	10	sccm

Fig. S1-1: Screenshot of a typical Savannah or MVD recipe for 100 cycles of (a) Al₂O₃ or (b) HfO₂.

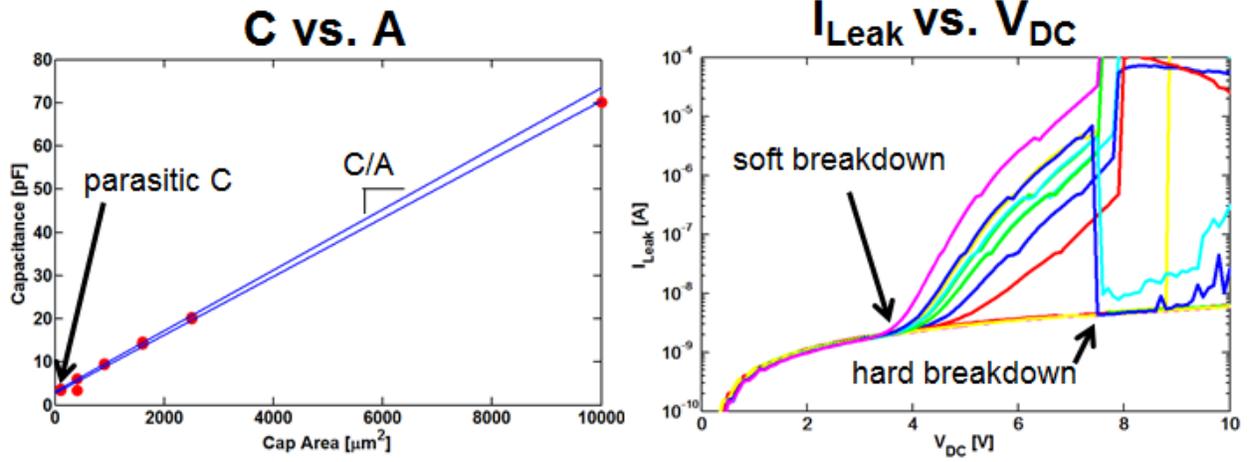
Shown below are recipes representative of all ALD processes performed for this study. The recipes in Fig. S1-1 happen to be for oxides deposited in the MVD at 125 °C, but the software and user interface is very similar between the Savannah and MVD systems. The critical step values for every recipe are:

- 1) all recipes were cycled between metal precursor and DI H₂O 100 times
- 2) 15 seconds of waiting time was inserted after each pulse to allow chamber pressure to stabilize
- 3) all TMA pulses were 0.03 s
- 4) all TDMA-Hf pulses were 0.3 s
- 5) all DI H₂O pulses were 0.03 s and 0.015 s for the MVD and Savannah, respectively

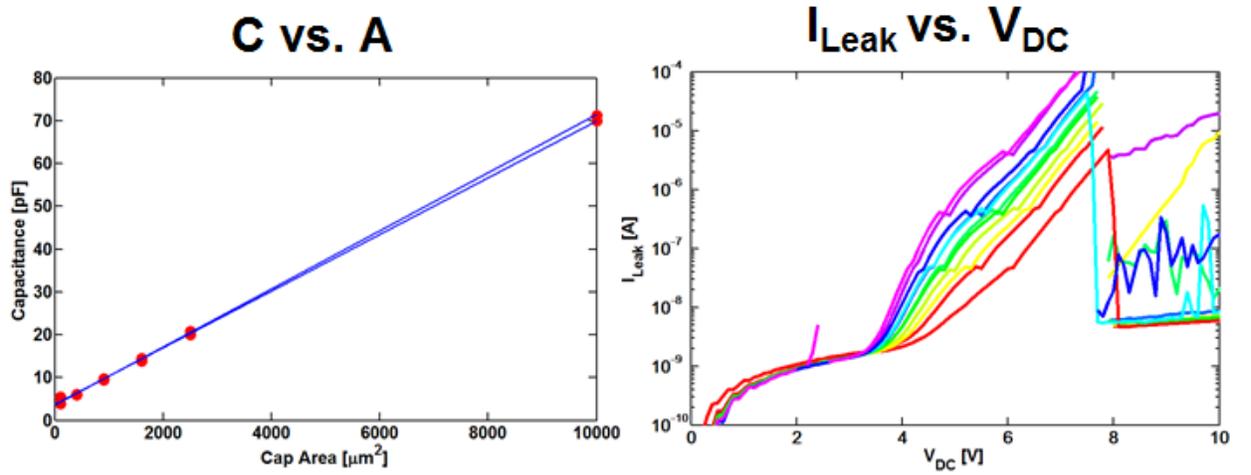
Appendix II – Data Fits for Benchmarked Oxides

Shown below are the data and fits of C vs. A for the oxides not featured in the main text of this report, as well as breakdown characteristics of the same.

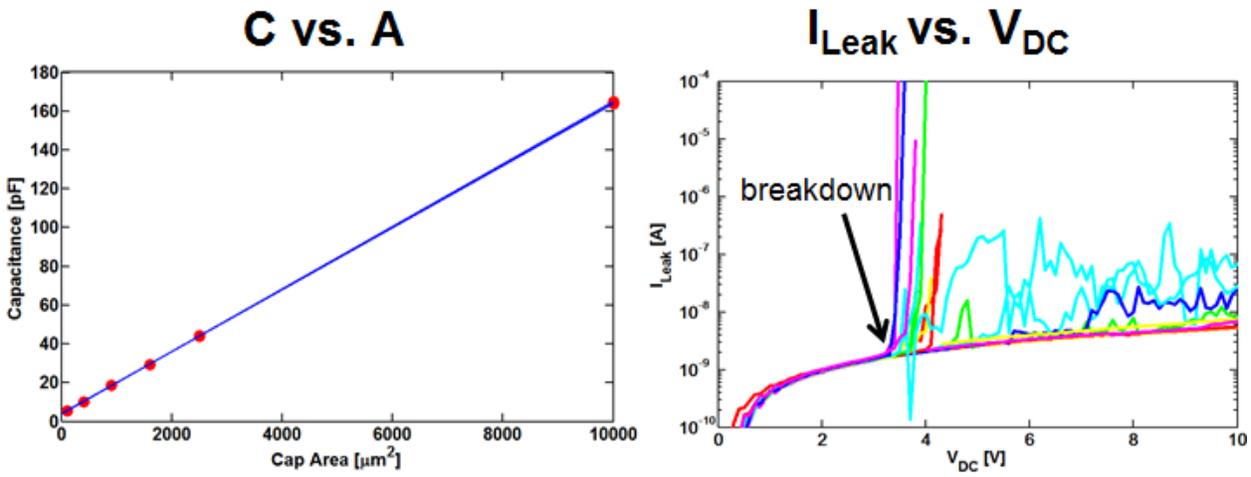
Savannah: 200 °C Al₂O₃ + 250 °C FGA



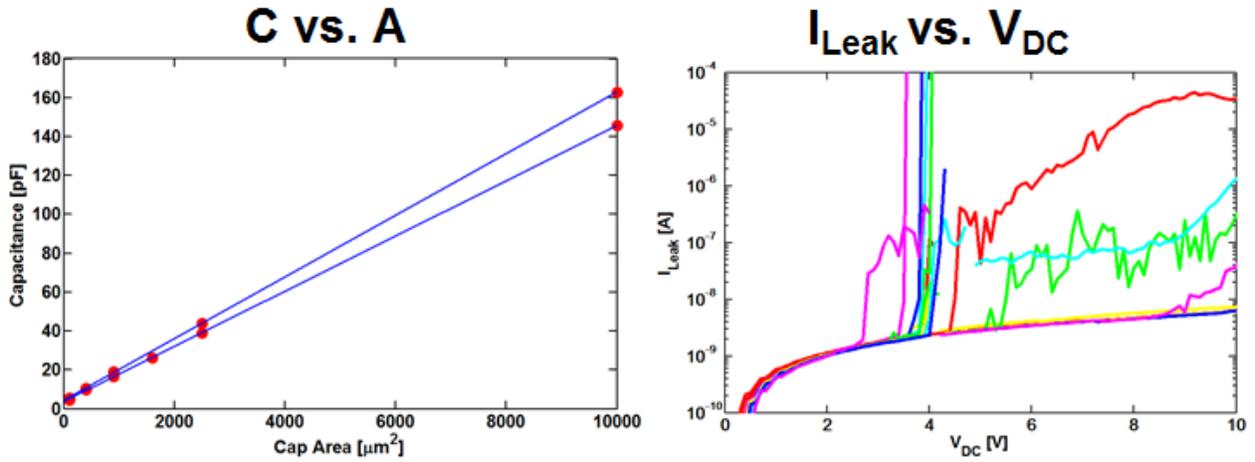
Savannah: 200 °C Al₂O₃ + 250 °C O₂ Anneal



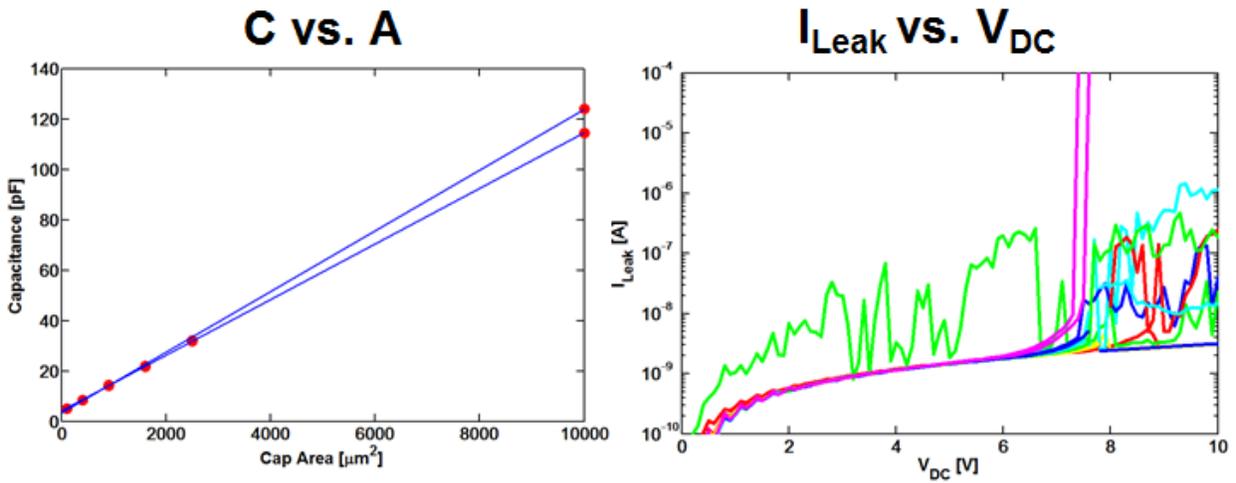
Savannah: 200 °C HfO₂ + 250 °C FGA



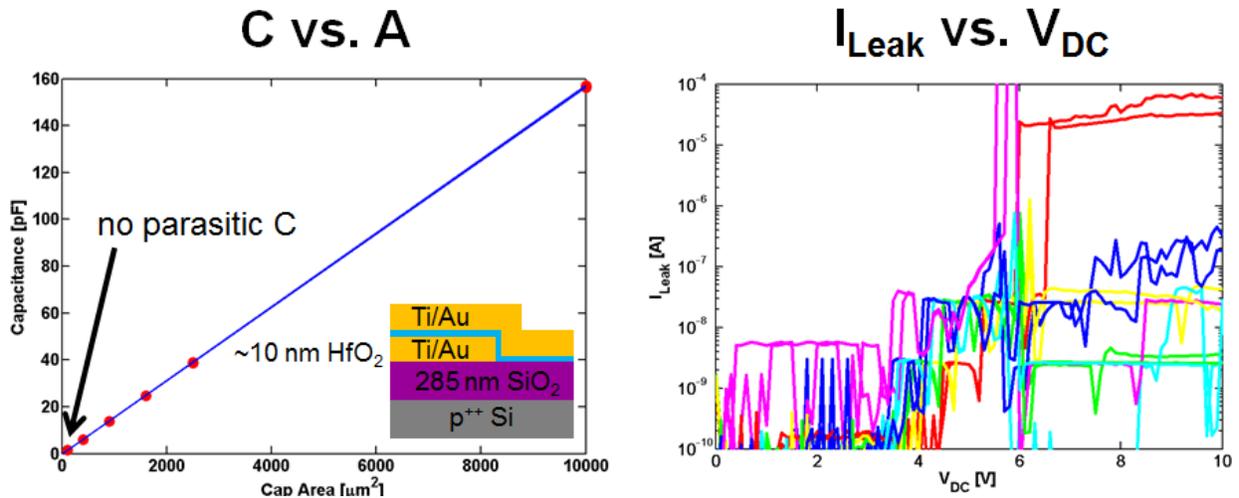
Savannah: 200 °C HfO₂ + 250 °C O₂ Anneal



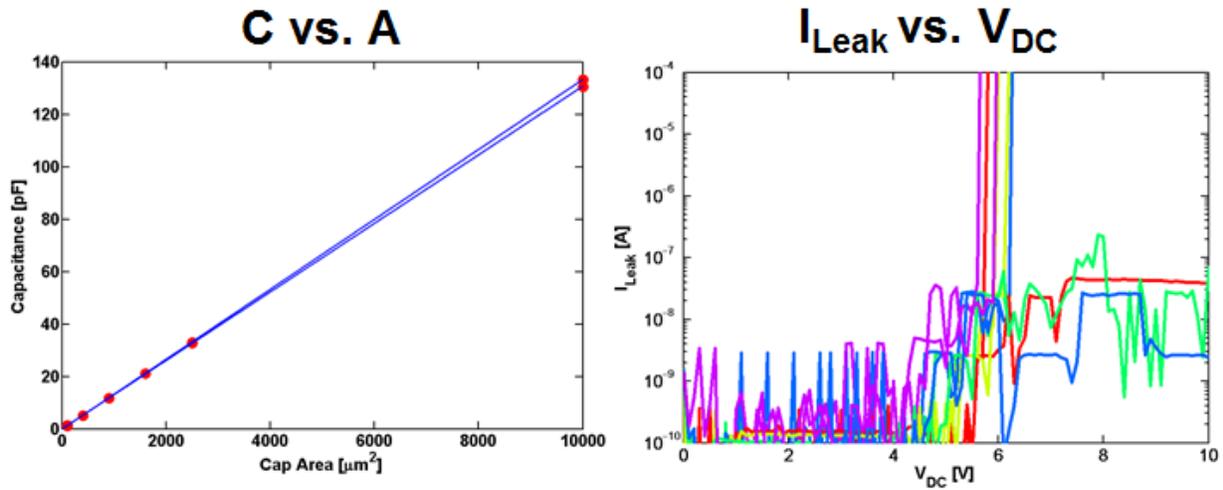
Savannah: 100 °C HfO₂ + 150 °C FGA



MVD: 125 °C HfO₂ + 125 °C FGA



MVD: 100 °C HfO₂ + 100 °C FGA



Appendix III – PDMS Thermal Integrity

Before lithography experiments were performed on PDMS, the thermal integrity of the PDMS itself was first briefly explored. PDMS “wafers” were produced by mixing PDMS and curing agent in a 10:1 ratio, thoroughly outgassing in vacuum for two hours, pouring ~20 grams into a clean fluoroware wafer holder lid, and curing at 80 °C for two hours (see Fig. S3-1). Using digital calipers, we measured the thickness of the wafer to be an average thickness of 3.46 mm. Following this, we diced the PDMS into five 1 × 1 cm pieces, heated them all on a hotplate at temperatures up to 300 °C, and measured their cross-sectional areas after 30 and 60 minutes of continuous heating.

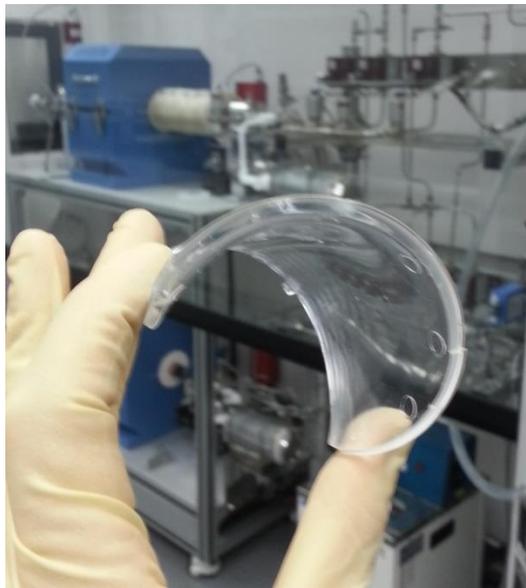


Fig. S3-1: A “wafer” of PDMS produced by pouring ~20 g of 10:1 PDMS:curing agent into a fluoroware lid for curing. The pieces cut from this wafer were ~3.5 mm thick and retained their shape unless deliberately bent.

Fig. S3-2 illustrates the results of our brief thermal integrity test. There is large uncertainty in our measurements due to the inherent flexibility of PDMS, but in general it can be said that, to within our conservative error estimates, all heating temperatures cause similar thermal expansion of about 10%. Furthermore, the area expansion can be seen to actually decrease slightly for temperature above 200 °C, which might be evidence of such extreme temperatures causing further curing of the PDMS, which would allow for less thermal expansion. Finally, it should be noted that at temperatures even up to 300 °C, the PDMS pieces retained their square shapes and suffered no visible damage.

This 10:1 PDMS cured at 80 °C was utilized for processing iterations 1 and 2 described in the “Dos and Don’ts” section above. For the third through sixth iterations, however, the PDMS and curing agent were mixed in a 5:1 ratio, poured into a clean fluoroware lid, thoroughly outgassed for two hours, and finally baked at 120 °C for two hours, in hopes of creating a stiffer product with a smaller coefficient of thermal expansion.

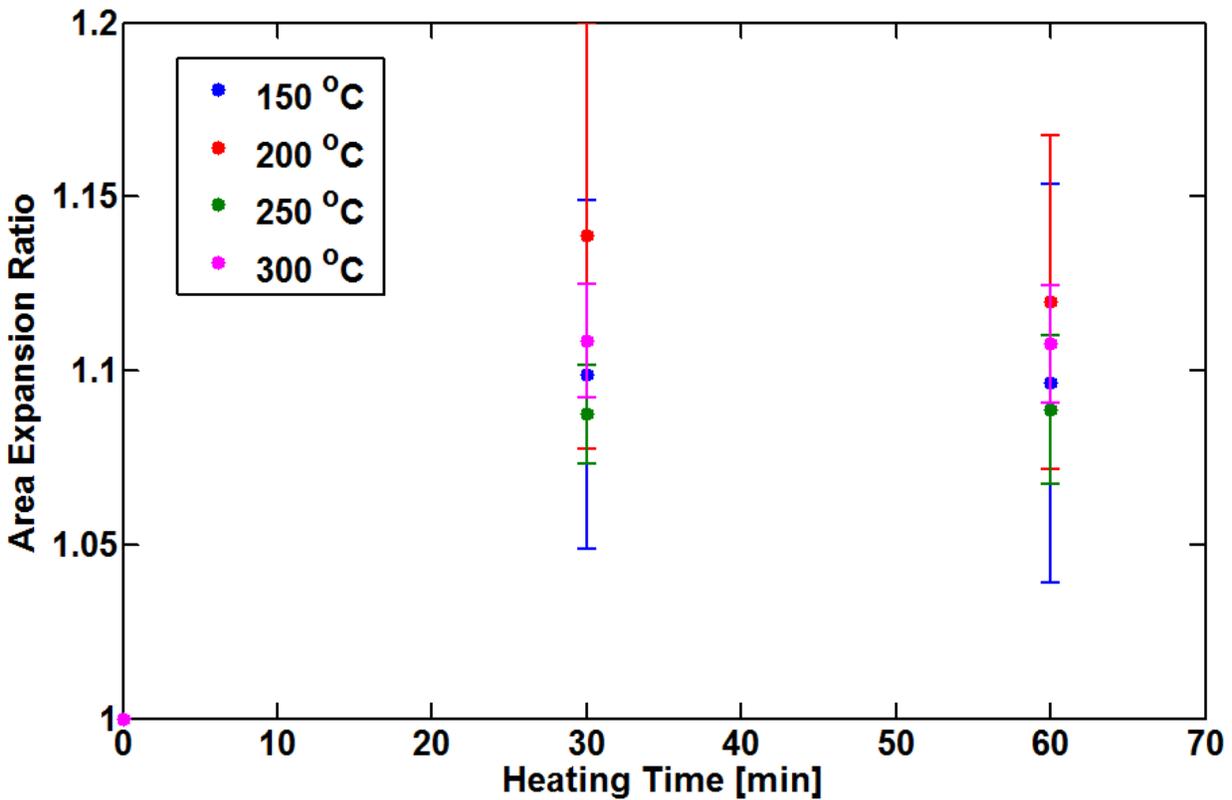


Fig. S3-2: Thermal integrity data for five pieces of 1 × 1 cm PDMS heated under various thermal budgets. All temperatures appeared to cause the PDMS to increase in area by approximately 10%, and little change was observed between 30 and 60 minutes of heating. Data points are the mean of the five pieces, while error bars reflect one standard deviation.

Appendix IV – Supplementary Update – 25 February 2016

Following the end of the 2015 Fall quarter, additional tests were performed to further investigate the top metal liftoff issues illustrated in Fig. 14, including using alternative top metals, different ALD recipes, and adding an interfacial buffer layer. It should also be noted that these further tests were performed on flexible electronics-grade PEN, which are considerably cleaner, smoother, and more transparent than the PEN tested previously. The exact type of PEN used was Teonex Q65HA, acquired from Teijin DuPont Films [7].

First and foremost, it should be stated that, for whatever reason, the Teonex PEN films cannot survive RTA processing, even at temperatures as low as 125 °C. The initial attempt to perform an RTA after high- κ deposition resulted in a puddle of metal and plastic. As such, additional tests were performed in parallel to verify the integrity of the dielectrics without annealing. All experiments performed hereafter were done only with hafnia deposited in the MVD, though it is expected that alumina will behave similarly.

The first experiment performed was depositing different metals for the top electrodes. To begin, four SiO₂/Si and four PEN substrates underwent the same lithography, metallization, and 100 cycles of 125 °C ALD processing that resulted in ~11.5 nm HfO₂ deposited on 2/38 nm Ti/Au electrodes. Subsequent lithography was then used to define top electrodes, and then one each of the four SiO₂/Si and PEN substrates was metalized with 10/30 nm Cr/Au, 20/20 nm Ti/Au, 40 nm Al, and 40 nm Ni. The post-liftoff results are shown in Figs. S4-1.

As can be seen, flawless liftoff was achieved for the HfO₂/SiO₂/Si substrates, regardless of top metal choice, while all top metals failed to stick on HfO₂/PEN. However, closer examination revealed that the top metal did stick only where it overlapped with the bottom electrodes. This observation strongly suggested that strain was somehow accumulating in the films during ALD that prevented additional metal layers from sticking, and indeed the Teijin website indicates that Teonex PEN shrinks by up to 0.4% when heated to 150 °C for 30 minutes. Although our processing only involved heating to 125 °C albeit for 60 minutes, the resulting strain was evidently substantial enough to cause processing problems.

Nevertheless, a few capacitors were measured on the SiO₂/Si substrates to examine how the properties of the hafnia might change without an annealing step, and these results are shown in Fig. S4-2. Regarding electrical properties, very little change is observed without RTA, the one exception being that the hafnia now experiences a weak breakdown near a field of 0.35 V/nm before hard breakdown. It should also be

noted that the measured capacitance values are extremely sensitive to the metals chosen for electrodes, as any native oxides that the metals form will contribute to a series capacitance. This is readily seen when comparing the measurements done for Al vs. Cr/Au top electrodes, with all other processing being exactly the same. For Al top metal, the capacitance per area was measured to be $1.16 \mu\text{F}/\text{cm}^2$, while for Cr/Au it was measured to be $1.32 \mu\text{F}/\text{cm}^2$, which lead to respective κ values of 15.1 and 17.2 for the exact same oxide. While it is known that both Al and Cr form surface oxides a few nm deep, the different native oxide thicknesses and dielectric constants of CrOx vs. AlOx is evidently enough to yield substantially different measurements. In light of this, it is very possible that the intrinsic dielectric constant of the hafnia itself is even higher than 17.2, but is extrinsically lowered due to the necessity of forming additional interfaces with electrical contacts.

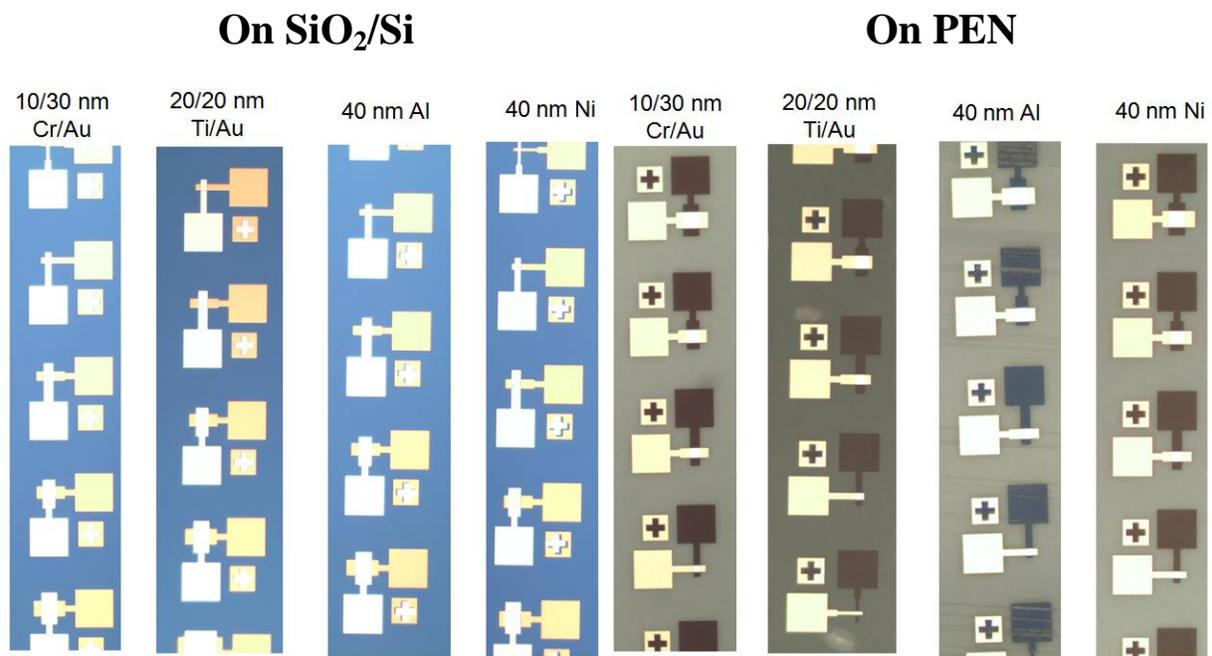
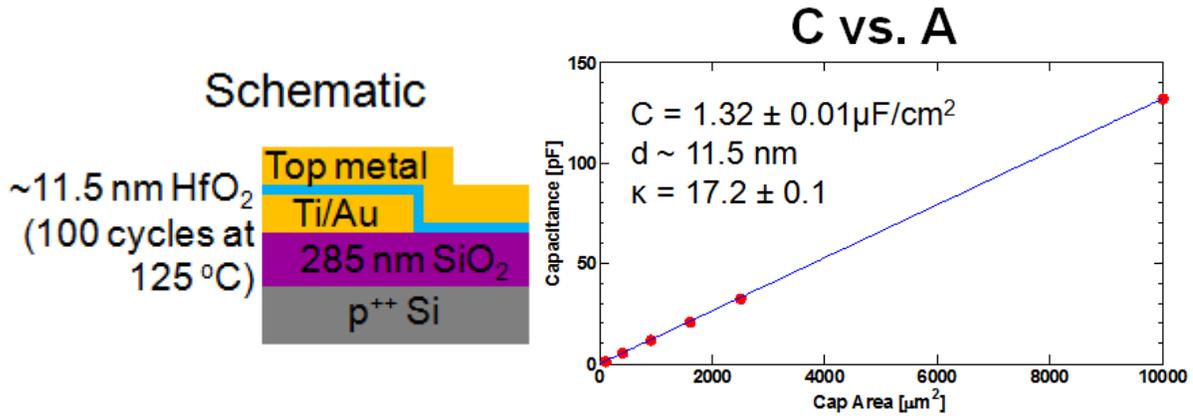


Fig. S4-1: Optical images of capacitor arrays on SiO₂/Si (left) and PEN (right). The device stack is: substrate / 2/38 nm Ti/Au / 100 cycles 125 °C MVD hafnia / top electrode. The top electrodes all stick on SiO₂/Si, but do not on PEN except where they overlap the bottom electrodes.

After confirmation that the oxides still functioned as intended without RTA, several approaches were tried simultaneously in an effort to mitigate the strain caused during the ALD process. These included depositing the hafnia for 100 cycles at 100 °C (to cause less strain), depositing 400 cycles of hafnia at 125 °C (to mitigate the strain through a thicker film), and depositing a 10 nm AlOx layer by ebeam evaporation *before* any subsequent processing was performed whatsoever for both aforementioned depositions. Optical images illustrating the results are shown in Fig. S4-3.

MVD: 125 °C HfO₂ + No RTA, 10/30 nm Cr/Au top contacts



MVD: 125 °C HfO₂ + No RTA, 40 nm Al top contacts

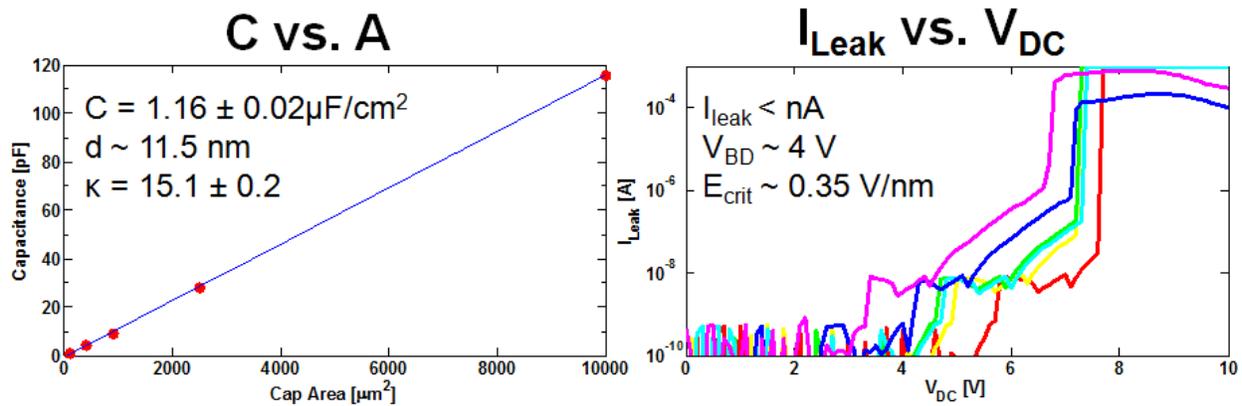


Fig. S4-2: Measurements of some devices shown in Fig. S4-1, with Cr/Au (top) and Al (bottom) top contacts. A larger capacitance value is extracted from the Cr/Au contacts, ostensibly due to a less detrimental contact-dielectric interface.

Both the lower deposition temperature and thicker films on PEN alone appear to help somewhat in reducing surface strain, but neither yields flawless electrode liftoff. However, for both of these deposition temperatures, inserting the 10 nm AlOx buffer layer allows for perfect liftoff with one caveat: these substrates cannot be sonicated, or else holes form in the AlOx buffer. The optical images for substrates with an AlOx buffer that were sonicated during the bottom electrode liftoff are shown in Fig. S4-3, and demonstrate the point very nicely that only in regions where the AlOx remained did the top electrodes stick completely. The AlOx thus acts as a double-edged sword, in that the weak interaction between the PEN and AlOx allows for little coupling of strain between the PEN and AlOx, but also means that any agitation such as sonication will cause delamination. We also note that it is important that the AlOx buffer is deposited by ebeam evaporation at room temperature, so that no strain is present in the PEN during this step.

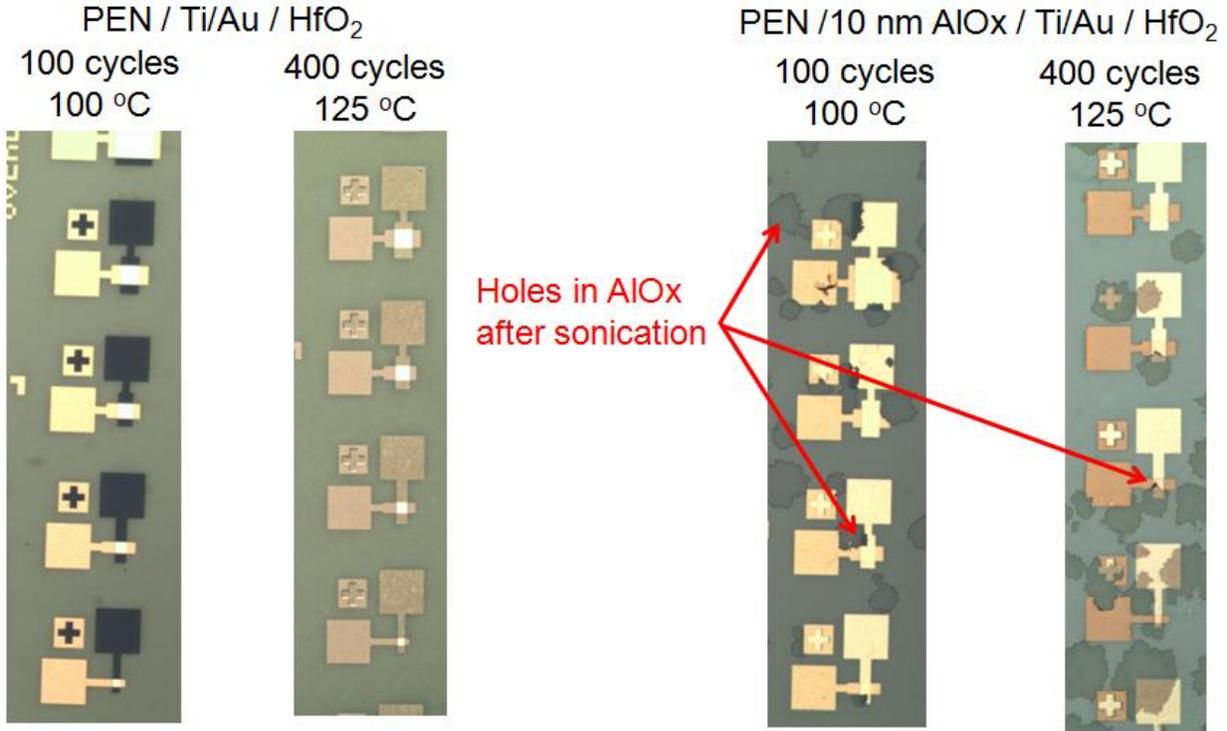


Fig. S4-3: Optical images of various approaches to reducing surface strain in ALD hafnia on PEN. Lower temperatures and thicker oxides were tried both with (right) and without (left) a 10 nm AlO_x buffer layer.

With such strong indicators that it was indeed the AlO_x buffer that allowed for clean top electrode liftoff, we returned to our original desired recipe of 100 cycles of hafnia at 125 °C. Both top and bottom electrodes were 2/38 nm Ti/Au, and the substrate was allowed to soak in Remover PG at room temperature for two hours after each metallization, to allow for easier liftoff by spraying with acetone. A schematic and picture of the resulting substrates can both be found in Fig. S4-4, along with a picture of metal cylinders used to strain the substrate.

An array of capacitors was first measured before any strain had been intentionally applied, though the substrate surely experienced some amount of strain during fabrication and routine handling. We then utilized cylinders to easily apply a known uniaxial strain, ϵ , around a radius of constant curvature, r :

$$\epsilon = -\frac{t}{2r}$$

where t is the thickness of the substrate. For cylinder diameters of 25.3 and 12.7 mm and a PEN thickness of 125 μm , the strains were very near to 0.5 and 1.0%, respectively. Compressive strain was not applied for fear of damaging the structures on the surface. Following 100 cycles of straining to 0.5% and 1.0%, a new set of capacitors was measured for both C-V and breakdown characteristics, all shown in Fig. S4-5.

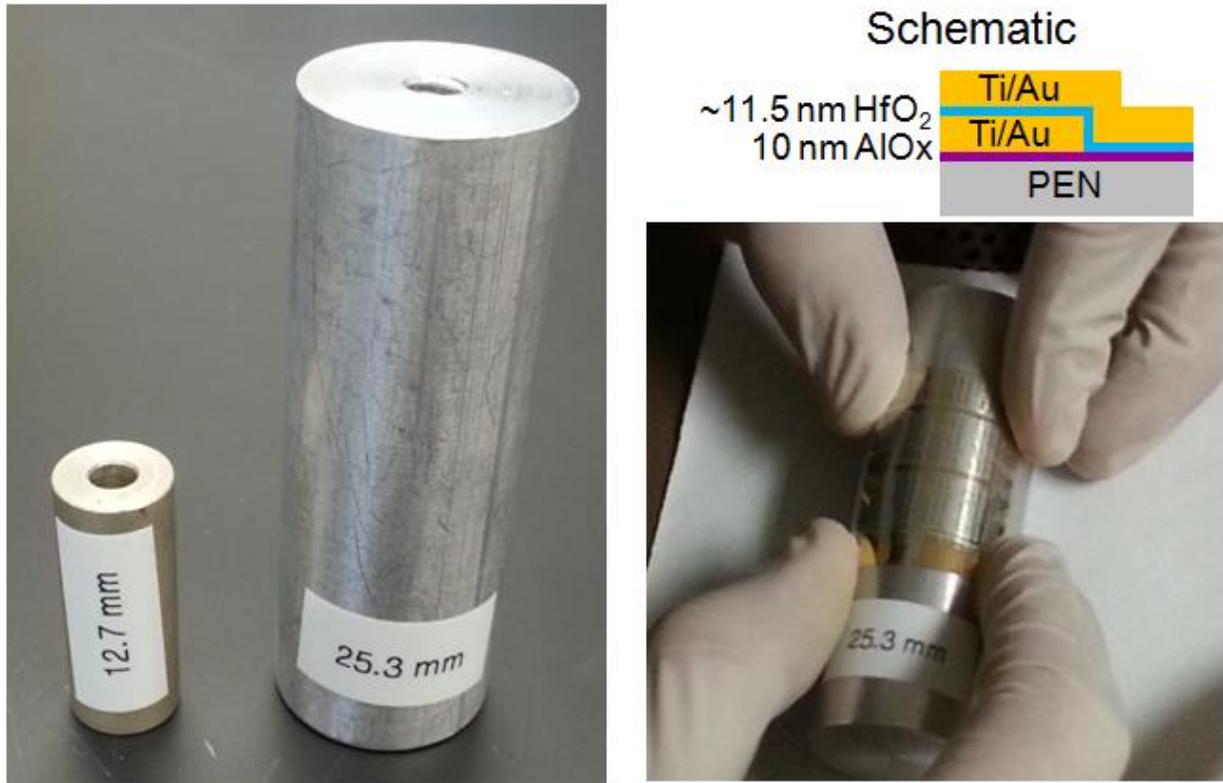
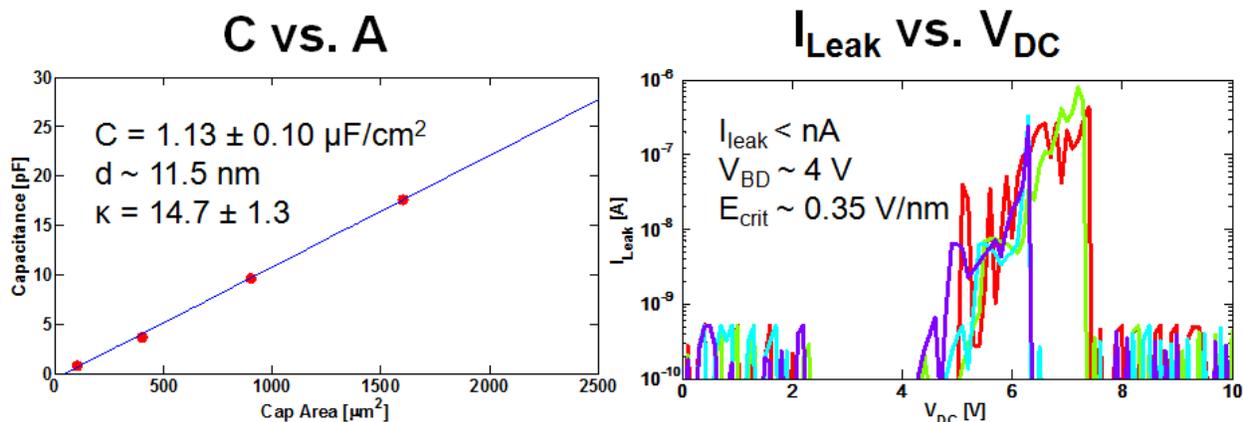


Fig. S4-4: Optical pictures of the two cylinders used to apply constant uniaxial strain across the entire substrate, and a demonstration of how this strain was applied. A schematic of the measured structures is also pictured.

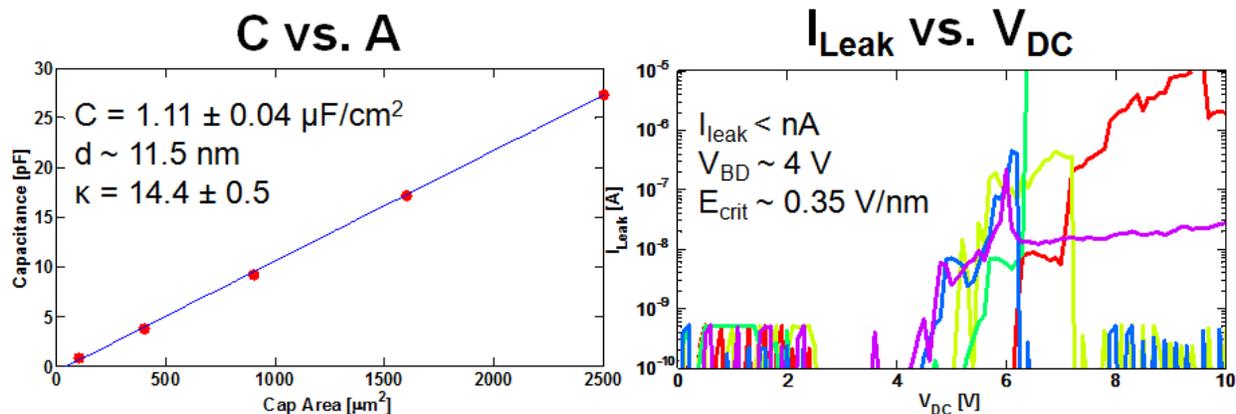
Interestingly, the dielectric properties of the hafnia with no intentional strain applied was significantly lower than what might be expected from Table 1. Whether this is due to unintentional strain caused by handling the substrate during fabrication, or whether the film grows on biaxially tensile strained PEN and so undergoes biaxial compression upon cooling, we can only speculate. Regardless, the capacitance value is still in excess of $1 \mu\text{F}/\text{cm}^2$, and the break down characteristics are similar to, if a little lower than, the values in Table 1. 100 cycles of 0.5% uniaxial strain seemed to have no effect on the characteristics of the hafnia, as the values extracted for C , κ , and E_{crit} are well within the error bars compared to 0 applied strain. However, after 100 cycles of 1.0% uniaxial strain, despite exhibiting exactly the same dielectric properties, the capacitors were found to become relatively leaky. This might suggest that the oxide retains its material properties under this level of strain but simply cracks into domains which allow for the flow of current, but this is again mere speculation.

Finally, we wish to note that the AlOx buffer layer also preserves the full transparency of the PEN (LOL 2000 and SPR 3612 tend to stain PEN yellow if applied directly, and cannot be undone even with extensive soaks in photoresist stripper and oxygen plasma treatments).

No Strain



0.5% Strain



1.0% Strain

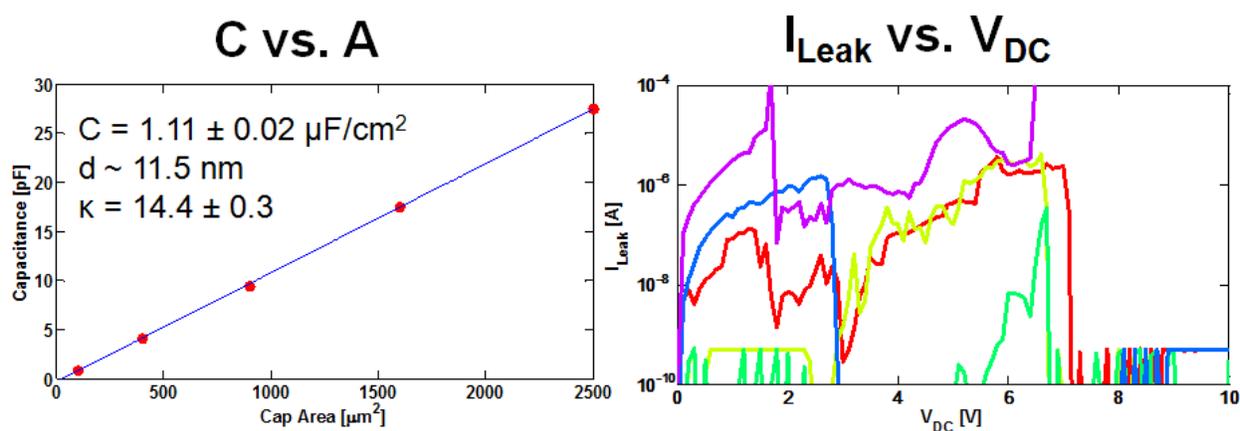


Fig. S4-5: C-V and breakdown characteristics of single capacitor arrays with 0, 0.5%, and 1.0% applied strain. All characteristics are preserved between 0 and 0.5% strain. Capacitance is preserved after 1.0% strain, but the oxides become extremely leaky.