Variable Trench Optimization for DRIE of SOI in PT-DSE

EE 412 Final Presentation

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STANFORD
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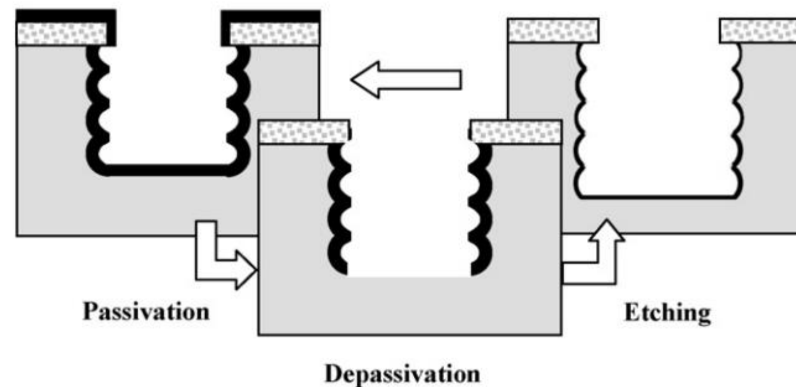
Outline

- Deep Reactive Ion Etching (DRIE)
  - Background
  - Etch Characteristics
    - Blowout
    - Scalloping
    - Taper
    - Aspect Ratio Dependency (ARD)
    - Notching
    - Grassing
- Results
  - Optimized bulk etch
  - SOI

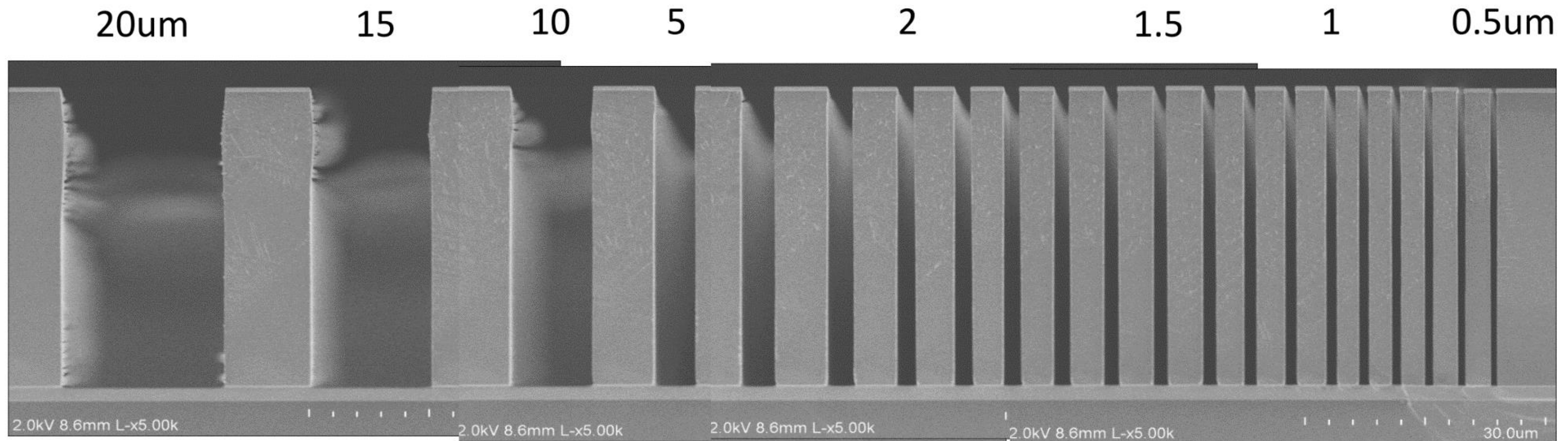
DRIE (Bosch etch)

- Passivation (Deposition)
  - Polymer deposition in C_4F_8
- Depassivation (Etch A)
  - High electrode bias etch of bottom polymer
- Etching (Etch B)
  - Silicon etch in SF_6



Bosch etch process
(Reza Abdolvand, Farrokh Ayazi)

University of Michigan – STS Pegasus



- Trench widths: 0.5 to 50 um
- Device Thicknesses: 20 and 40 um

DRIE characteristics

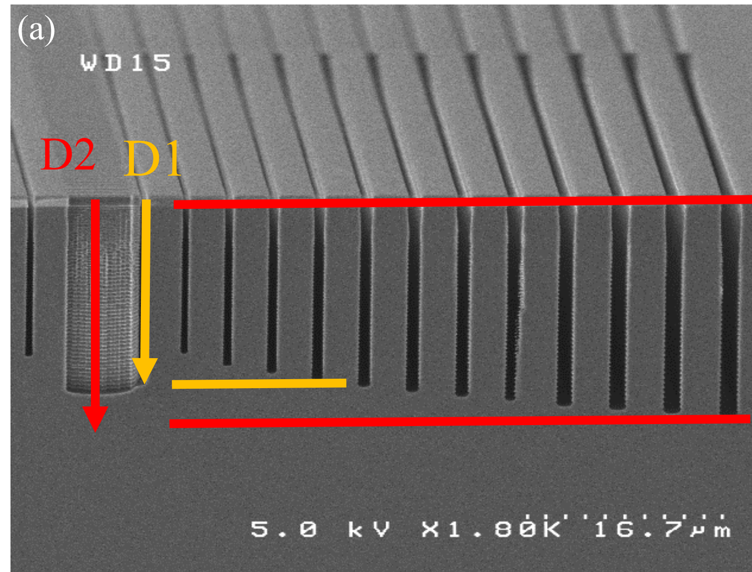
- Aspect Ratio Dependence (ARD)
  - Etch rate varies with trench size
- Blowout (undercut)
  - Lateral etching underneath mask
- Scalloping
  - Nonuniform etch due to three cycle process
- Tapering
  - Slower etch rate deeper in trench
- Notching (footing)
  - Lateral etching at silicon-insulator interface caused by charging
- Grassing
  - Unetched passivation polymer acts as masking feature during the etch step

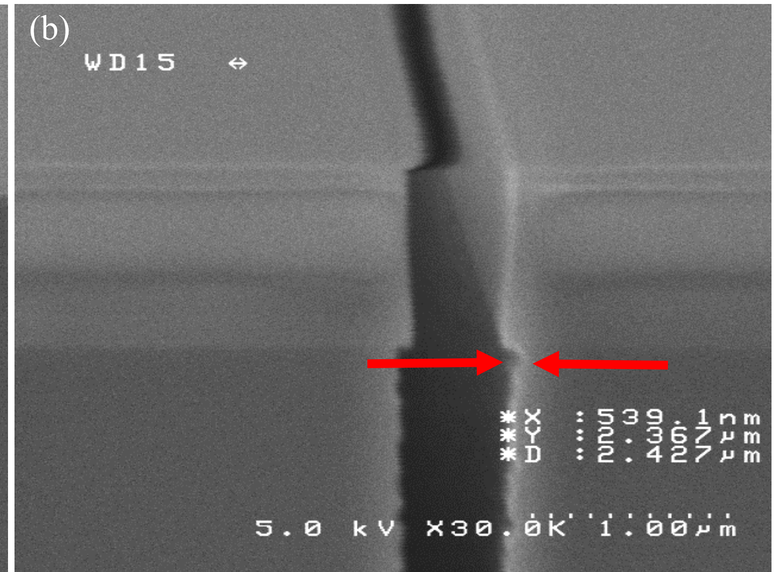
a) Aspect Ratio Dependence (ARD)

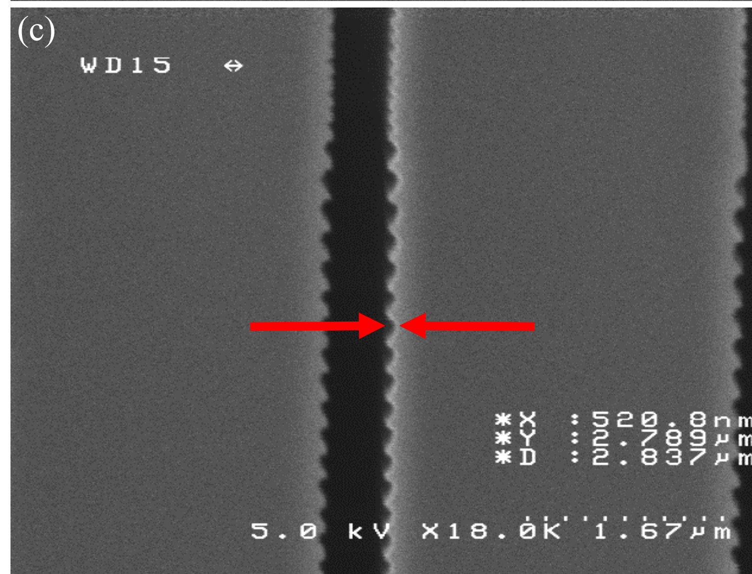
b) Blowout (Undercut)

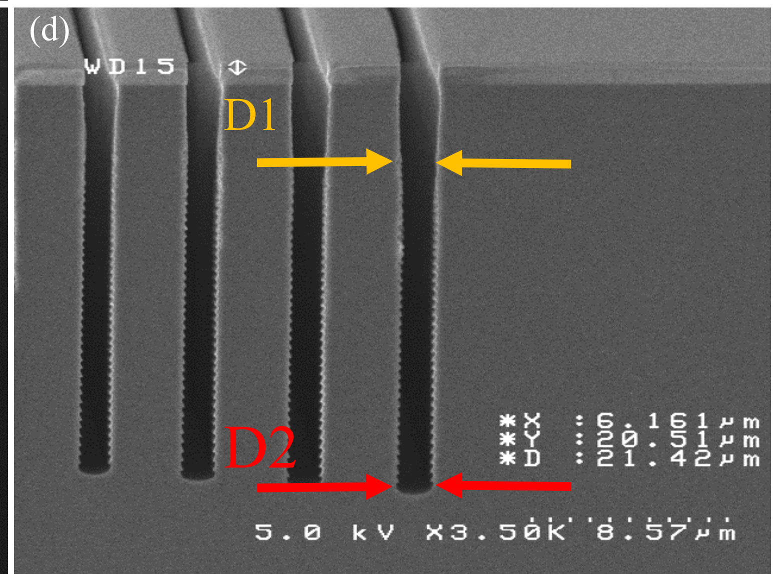
c) Scalloping

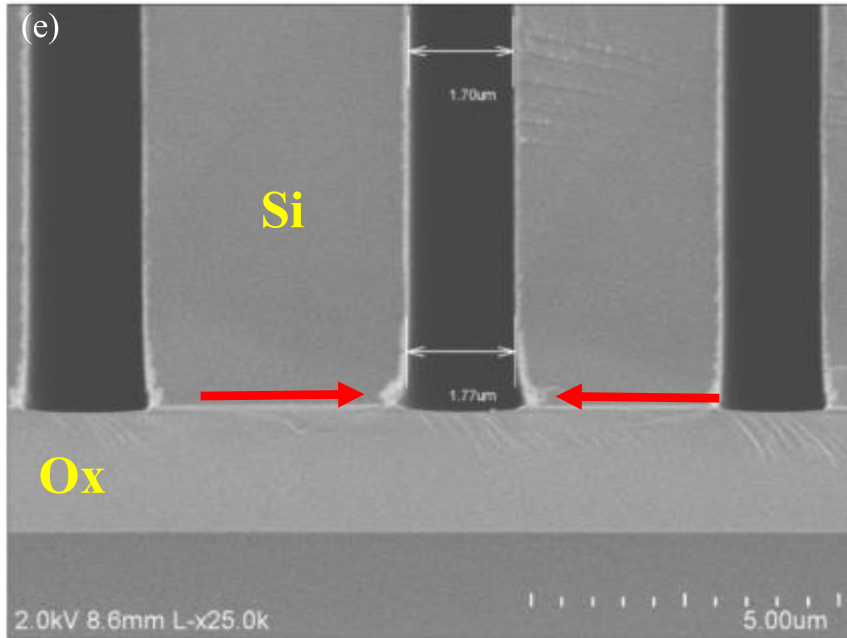
d) Tapering



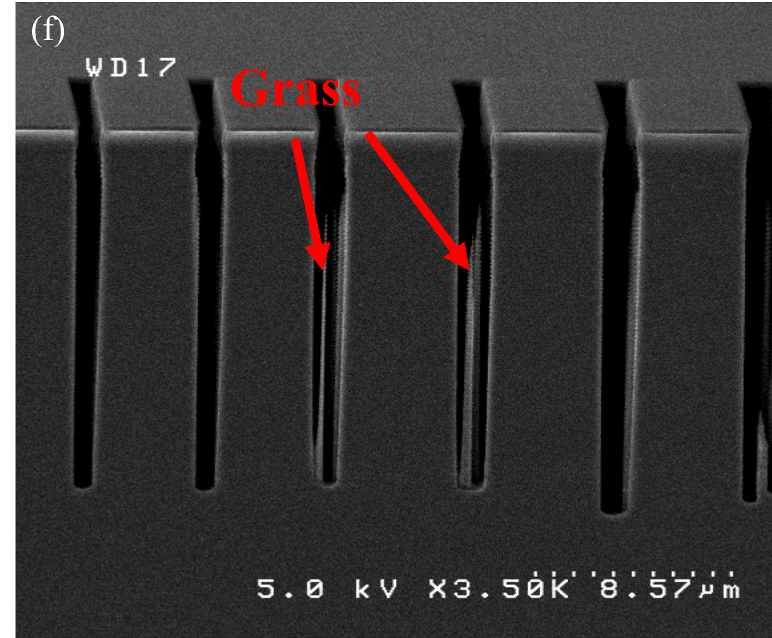








e) Notching



f) Grassing

DRIE characteristics

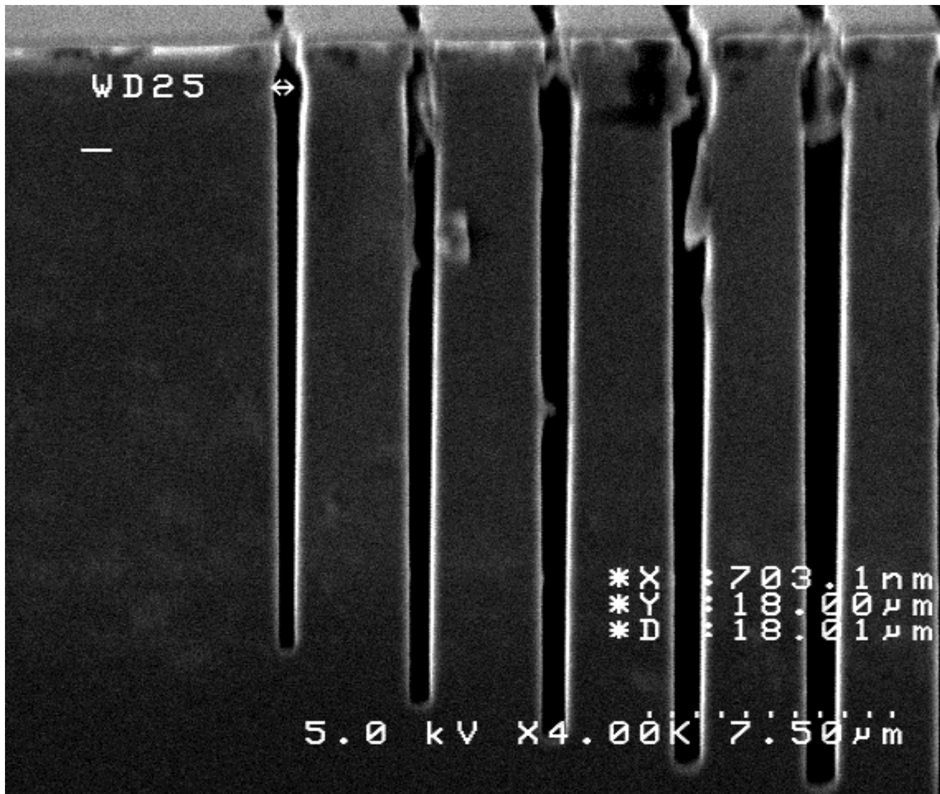
<u>Tradeoffs necessary</u>

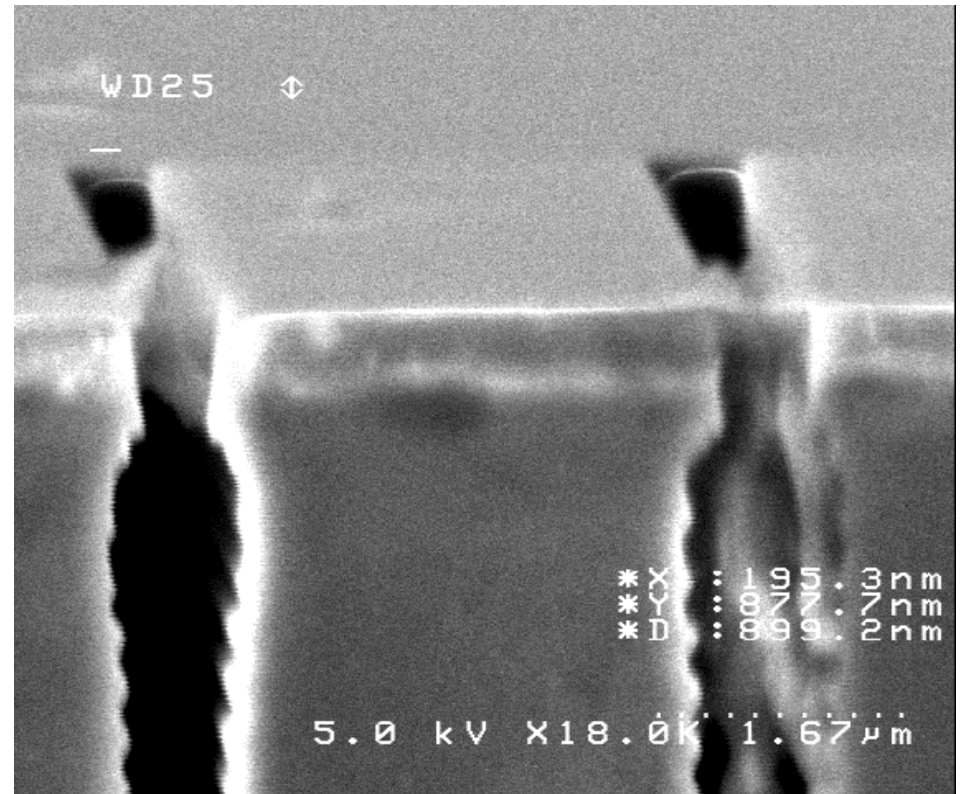
- Grass/blowout
  - Inversely related
- Grass/sidewall roughness
  - Inversely related
- Blowout/sidewall roughness
  - Related

Variable Increased	Etch Rate	Sidewall Roughness	Feature Blowout	Grass	Photoresist Selectivity	Polymer Breakdown
Etch gas	↑	↑	↑	↓	↑	↑
Dep gas	↓	↓	↔	↑	↑	↓
Etch:Dep time ratio	↑	↑	↑	↓	↔	↔
Pressure	↑	↑	↑	↓	↑	↑
Etch coil power	↑	↑	↑	↓	↑	↑
Dep coil power	↓	↓	↓	↑	↔	↓
Platen power	↔	↔	↔	↓	↓	↔
Etch EM1 value	↓	↔	↓	↔	↑	↓
Etch EM1 delay time	↔	↔	↔	↓	↓	↔

SNF Wiki – STS2 etch characteristics

Yushi-SOI-HAR





JMP– Design of Experiment (DOE)

- We designed a **screening** DOE to find out the region of interest.

	Pattern	Temperature	EtchA Bias Voltage	EtchB Bias Voltage	ARD	Blowout	Scalloping	Taper
1	+−−	1	-1	-1	•	•	•	•
2	−++	-1	1	1	•	•	•	•
3	−+−	-1	1	-1	•	•	•	•
4	+−+	1	-1	1	•	•	•	•
5	++−	1	1	-1	•	•	•	•
6	−−+	-1	-1	1	•	•	•	•
7	+++	1	1	1	•	•	•	•
8	−−−	-1	-1	-1	•	•	•	•

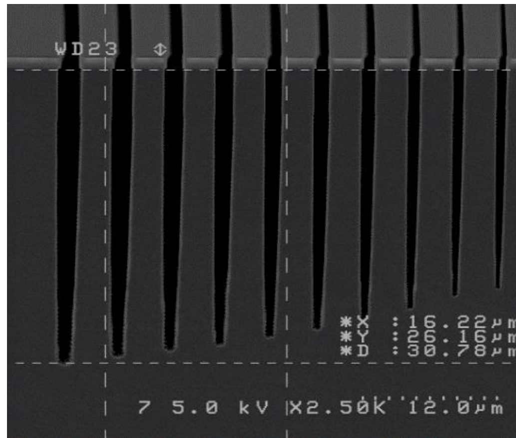
- Responses
  - Aspect Ratio Dependence (ARD)
  - Blowout
  - Scalloping
  - Taper
- Factors

  Temperature

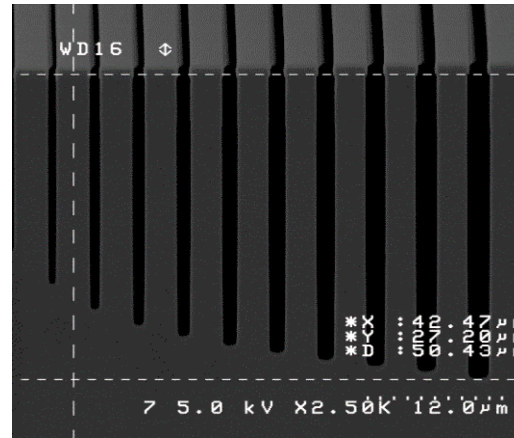
  EtchA Bias Voltage

  EtchB Bias Voltage

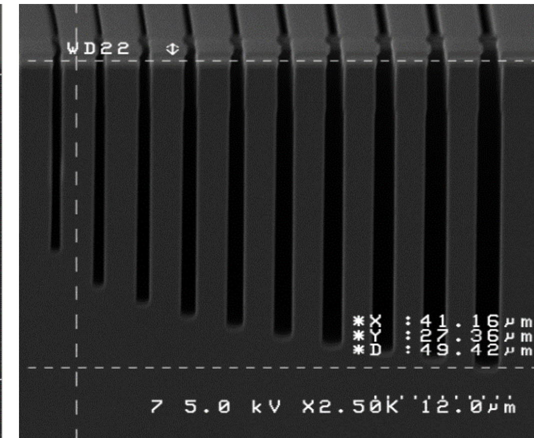
JMP – Design of Experiment (DOE)



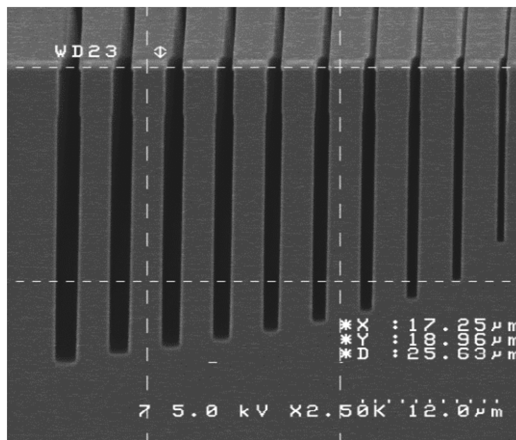
DOE: 30C -200V-10V



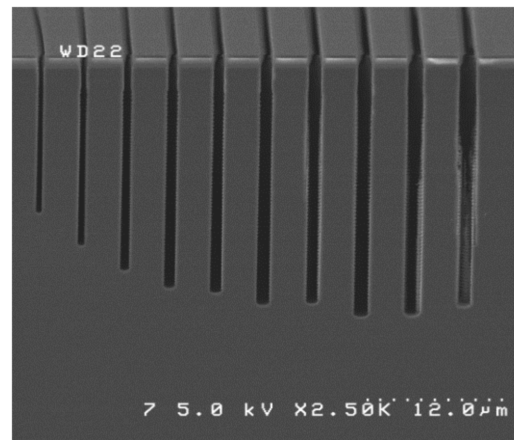
DOE: 30C-200V-150V



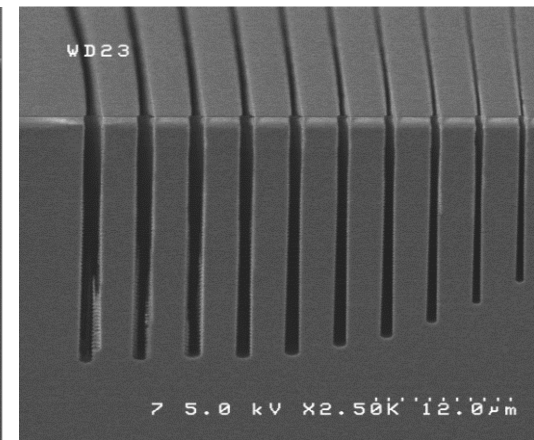
DOE: 30C-300V-150V



DOE: 30C-300V-10V



DOE: 0C-300V-10V



DOE: 0C-300V-150V

- Temperature
  - 30C/0C
- Etch A
  - 300V/200V
- Etch B
  - 150V/10V

Design of Experiment (DOE) Results

	Pattern	Temp	EtchA	EtchB	ARD	Blowout	Scalloping	Taper
1	"+--"	30	200	10	1.30	252	111	1.32
2	"-++"	0	300	150				
3	"-+-"	0	300	10	N/A	50	N/A	N/A
4	"+-+"	30	200	150	1.33	202.9	62.5	1.06
5	"++-"	30	300	10	1.39	128.9	128.9	1.12
6	"--+"	0	200	150				
7	"+++"	30	300	150	1.37	134	134	1.06
8	"---"	0	200	10				

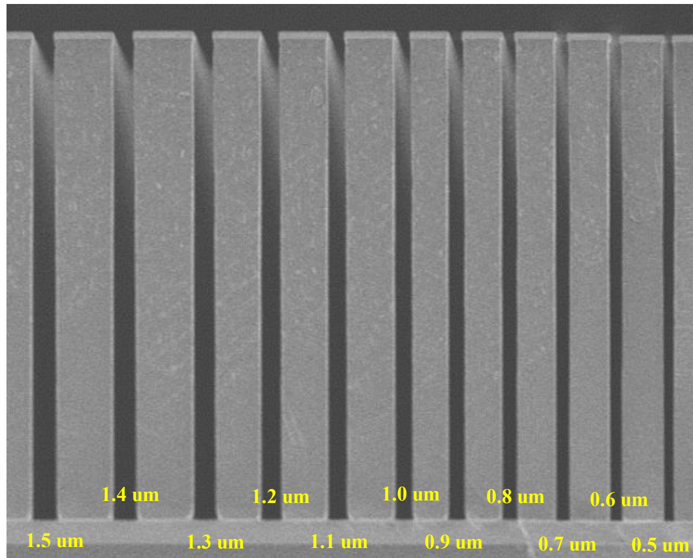
GRASS!!

- Full optimization difficult due to grassing
- Optimization region found
- Further fine tuning performed

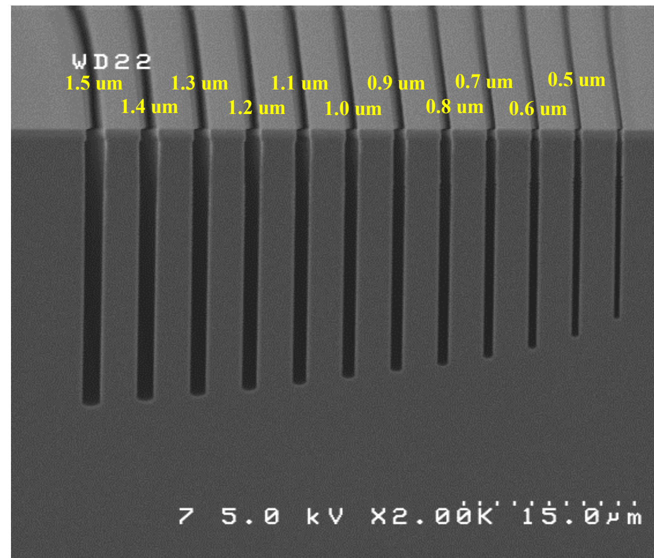
Fine tuning

- Tapering
  - Ramping
    - ↑ etch time
    - ↓ dep time
- Blowout
  - ↓ etch time
  - ↑ dep time
  - ↓ etch power/bias

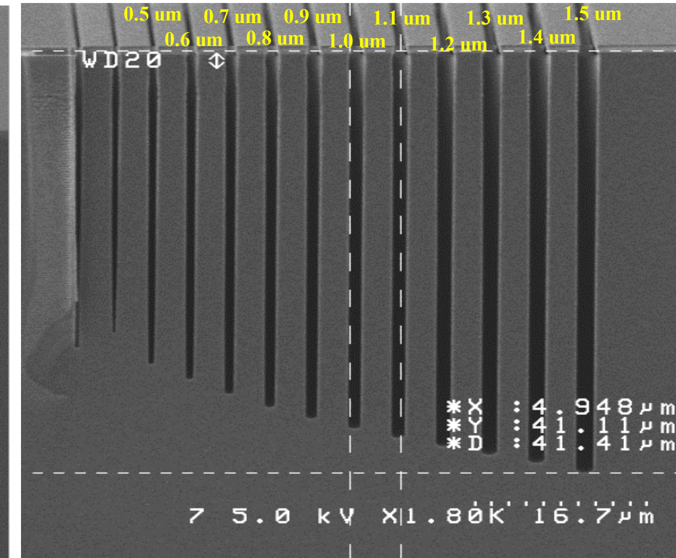
Variable trench comparison – STS Pegasus/PT-DSE



Michigan – STS Pegasus, 40 um depth



Stanford – PT-DSE, 20um depth



Stanford – PT-DSE, 40um depth

Variable trench comparison – STS Pegasus/PT-DSE

Stanford

Depth	ARD	Blowout (nm)	Scalloping (nm)	Taper
20um	1.23	169.0	< 100	1.03
40um	1.23	168.6	107.0	1.10

Michigan

Depth	ARD	Blowout (nm)	Scalloping (nm)	Taper
40um	N/A	150.0	< 100	1.15

- Comparable results between three recipes
- Variable bulk etch for PT-DSE ready
- SOI finish etch recipe required

SOI recipe (20um device layer)

- Loop 1
  - Slow, gentle etch to reduce blowout
- Loop 2
  - High power etch with ramping to provide sufficient etch rate for HAR trenches
- Loop 3
  - Slow, gentle etch with pulsing to reduce notching during over etch
  - Recommended by Plasma-Therm

Loop 1 – No. of cycles = 20

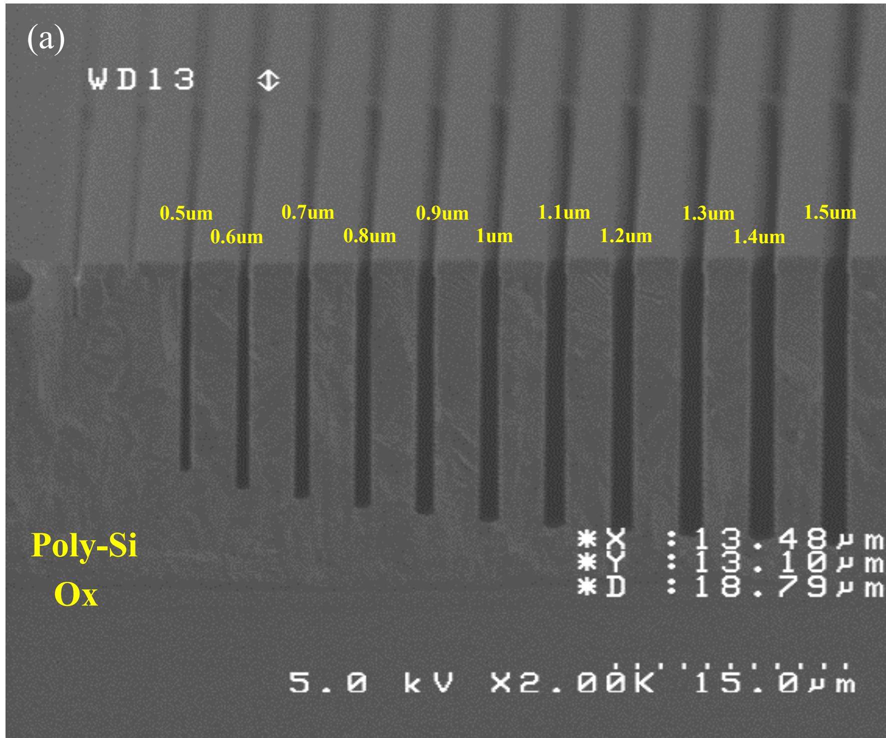
Parameter	Dep	Etch A	Etch B
C4F8 sccm	150	to pump	to pump
SF6 sccm	*150 to pump*	150	30
Ar sccm	30	30	30
Pressure	30	35	40
ICP watts	1500	1500	1500
V p-p	10	250	10
waveform	1	1	1
Step time (s)	1.5	1	1

Loop 2 – No. of cycles = 34

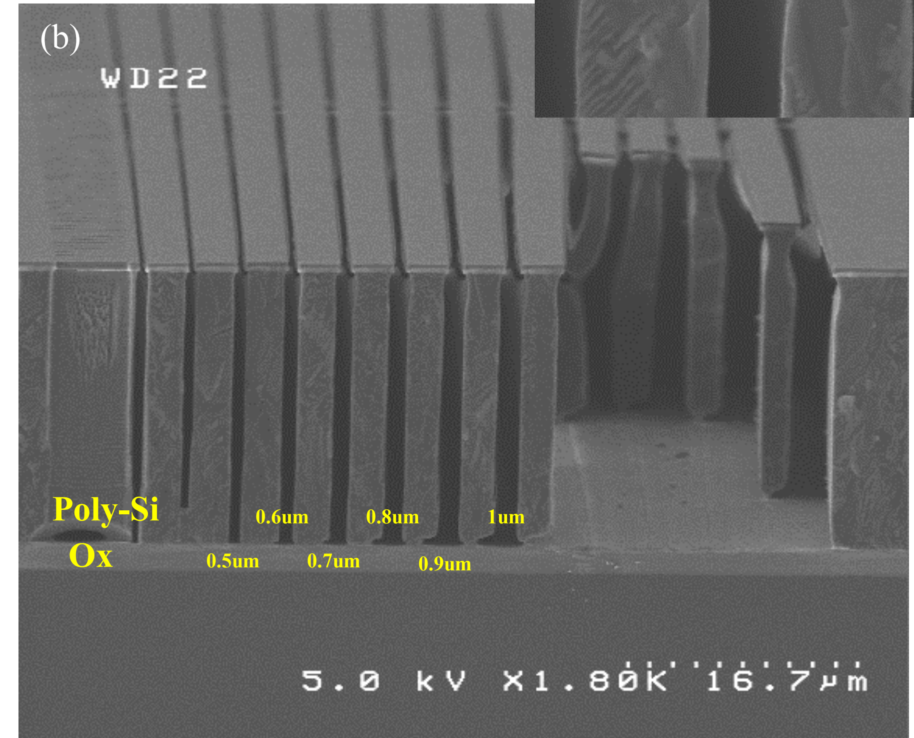
Parameter	Dep	Etch A	Etch B
C4F8 sccm	150	to pump	to pump
SF6 sccm	*150 to pump*	150	250
Ar sccm	30	30	30
Pressure	25	40	60
ICP watts	2000	2000	2000
V p-p	10	250	100
waveform	1	1	1
Step time (s)	2.3	1	1.5

Loop 3 – No. of cycles = 90

Parameter	Dep	Etch A	Etch B
C4F8 sccm	125	15	15
SF6 sccm	*75 to pump*	75	100
Ar sccm	30	30	30
Pressure	20	20	20
ICP watts	1600	1250	1250
V p-p	10	400	215
waveform	3	3	3
Step time (s)	2	2	1.5



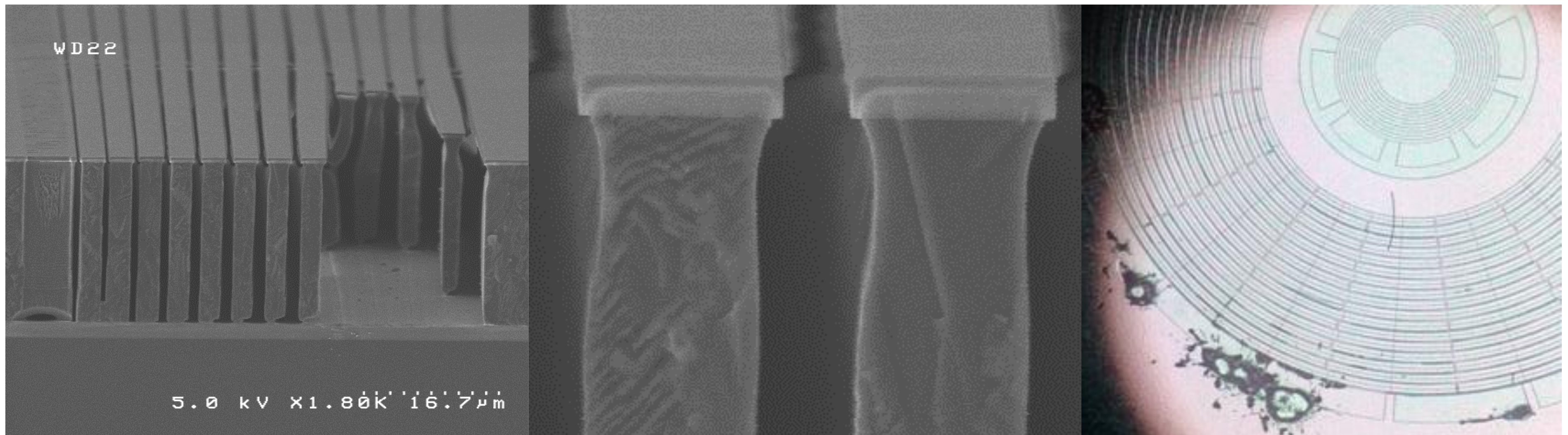
(a) Bulk etch on Polysilicon on Insulator. Loop 1 – 20 cycles; Loop 2 – 34 cycles



(b) Bulk and insulator etch on Polysilicon on Insulator. Loop 1 – 20 cycles; Loop 2 – 34 cycles; Loop 3 – 90 cycles

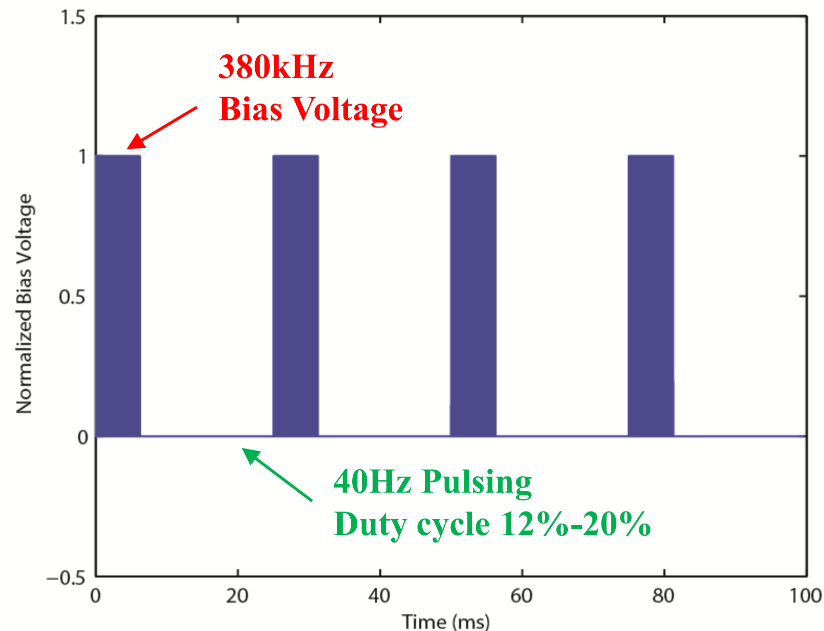
SOI issues in PT-DSE

- Etch issues observed upon 3rd pass
- Pulsing waveform dysfunction
  - Notching
  - Bowing (enhanced blowout)
  - Photoresist burnt



Low frequency bias pulsing reduces notching

- Bias pulsing reduces ionic charging of the oxide layer below the silicon device layer by allowing charge to dissipate during the pulsing "off" time.[1-2]
- STS2 has low frequency (380kHz) bias voltage and 40Hz pulsing with duty cycle of 12%-20%

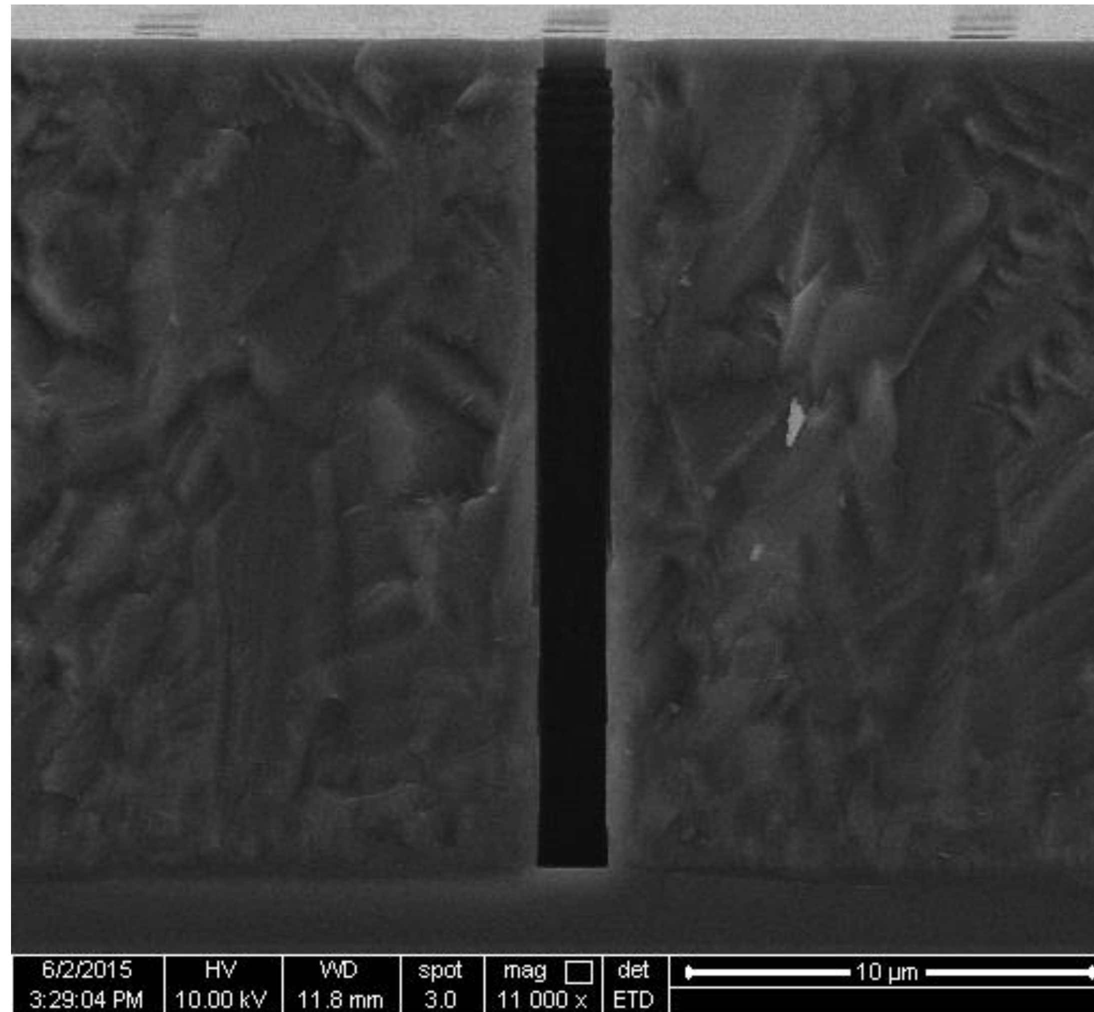


[1] M. Wasilik and A.P. Pisano, "Low frequency process for silicon on insulator deep reactive ion etching," Proc. SPIE, 4592, 462-472 (2001).
[2] K. Yonekura, M. Kiritani, S. Sakamori, T. Yokoi, et al, "Effect of charge build-up of underlying layer by high aspect ratio etching," Jpn. J. Appl. Phys., 37, 2314-2320 (1998).

Current PT-DSE status

- PT-DSE should be able to provide a 100kHz bias voltage with pulsing. Duty cycle of pulsing can be selected as 25% (waveform 2) and 15% (waveform 3) .
- PT-DSE currently cannot generate expected pulsing waveform.
- Aside from the waveform problems there exists a 50 Vpp RF noise signal which goes on and off on the bias line.
- Jim McVittie is working on fixing the waveform to match the STS2 waveform.
- We provided Plasma-Therm with Poly-SOI wafers for an etch demo. Further recipe development will be continued upon the demo results and repair of the tool.

Results
SEM Images – 1.5 µm Trench



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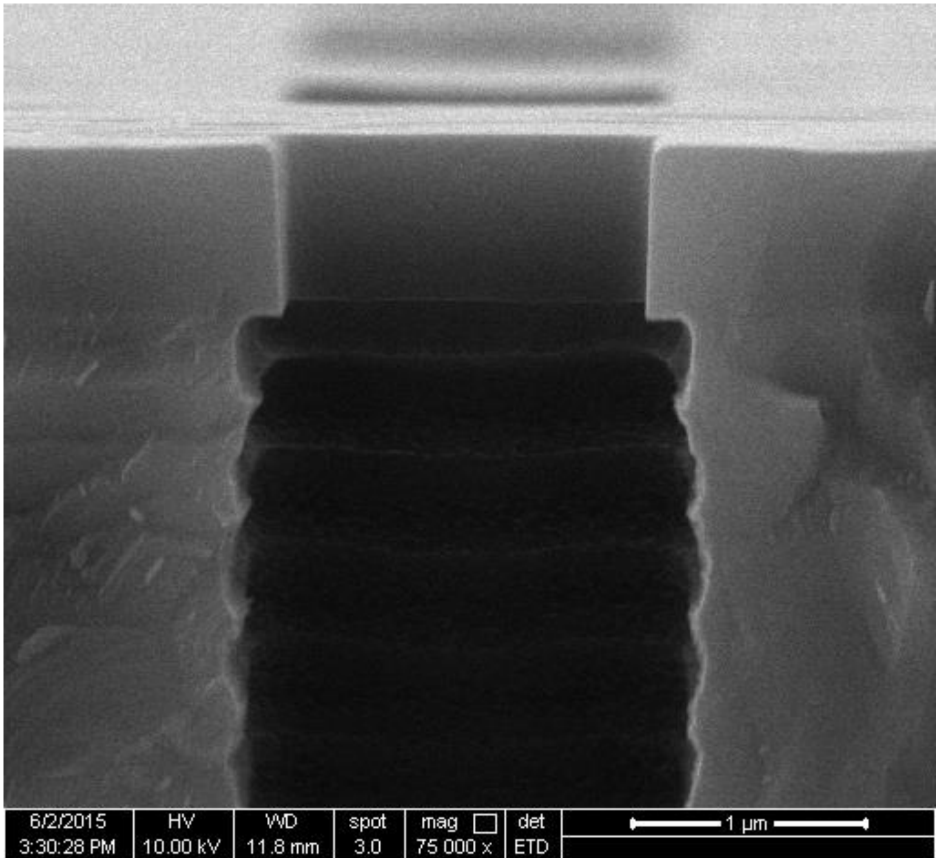

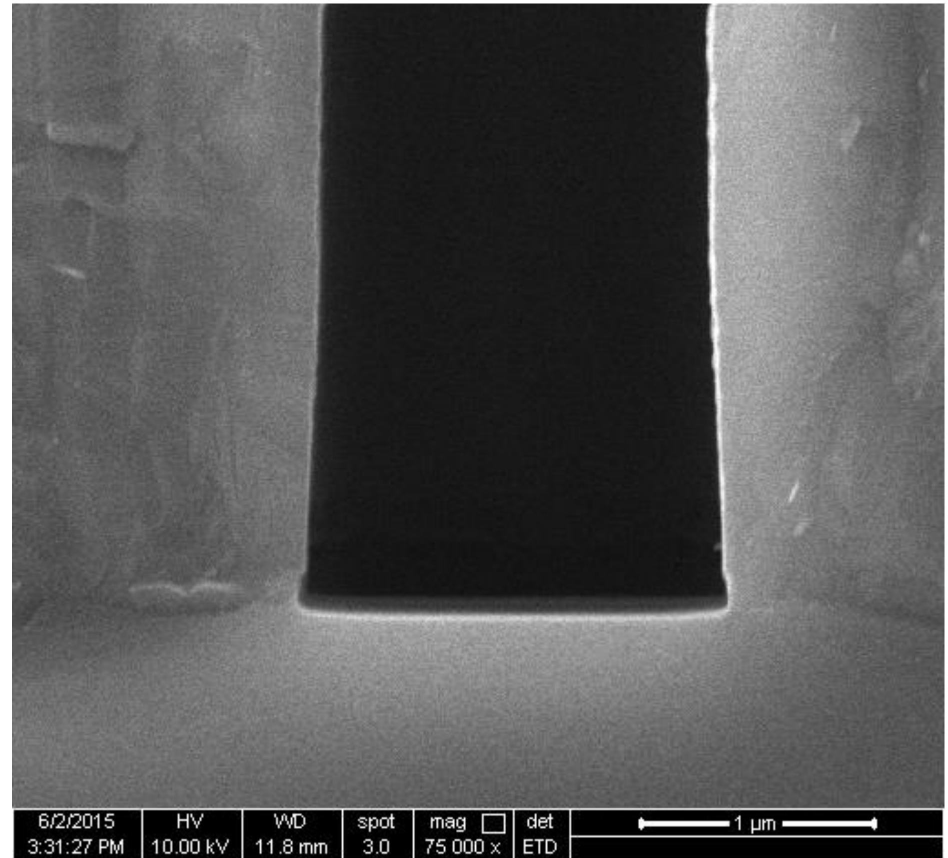

Results

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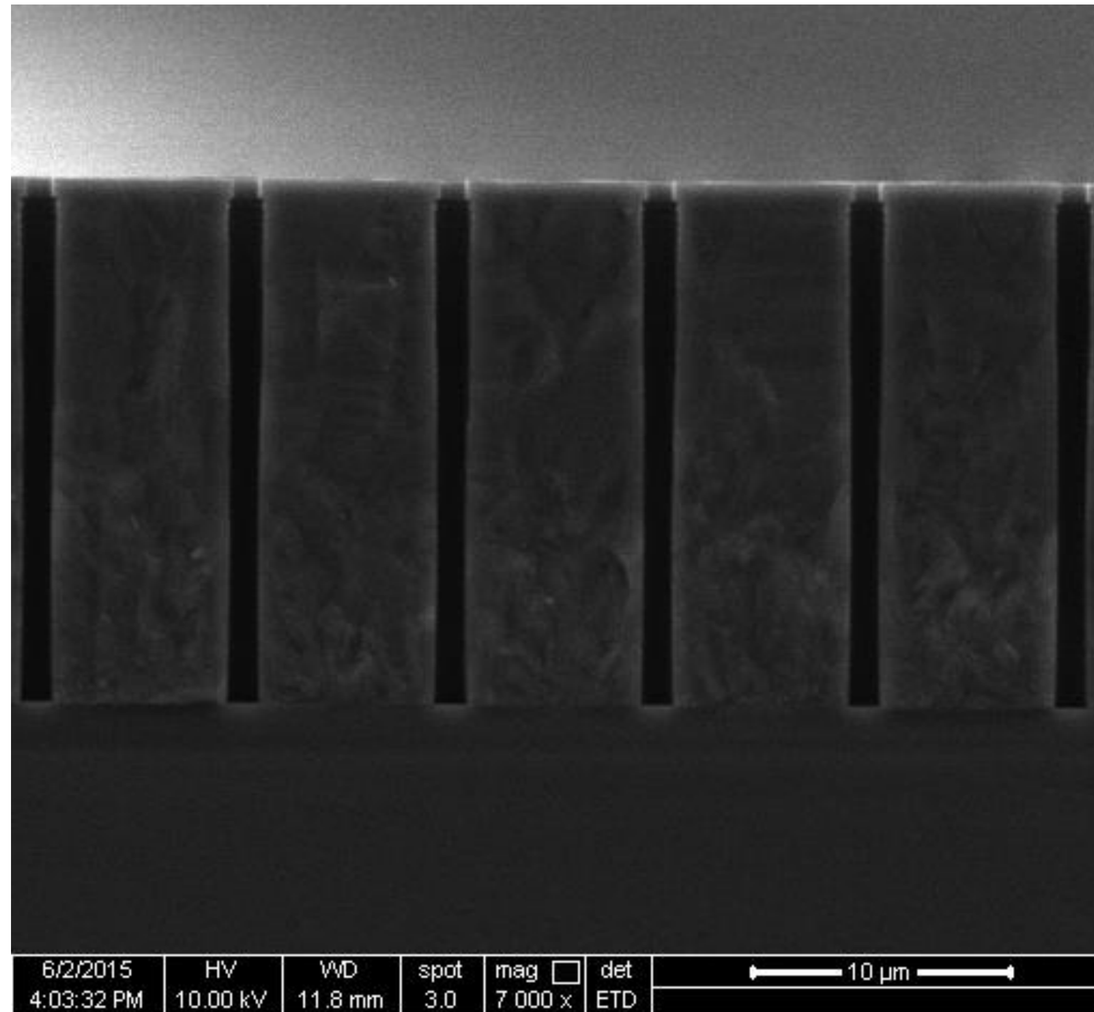

Results

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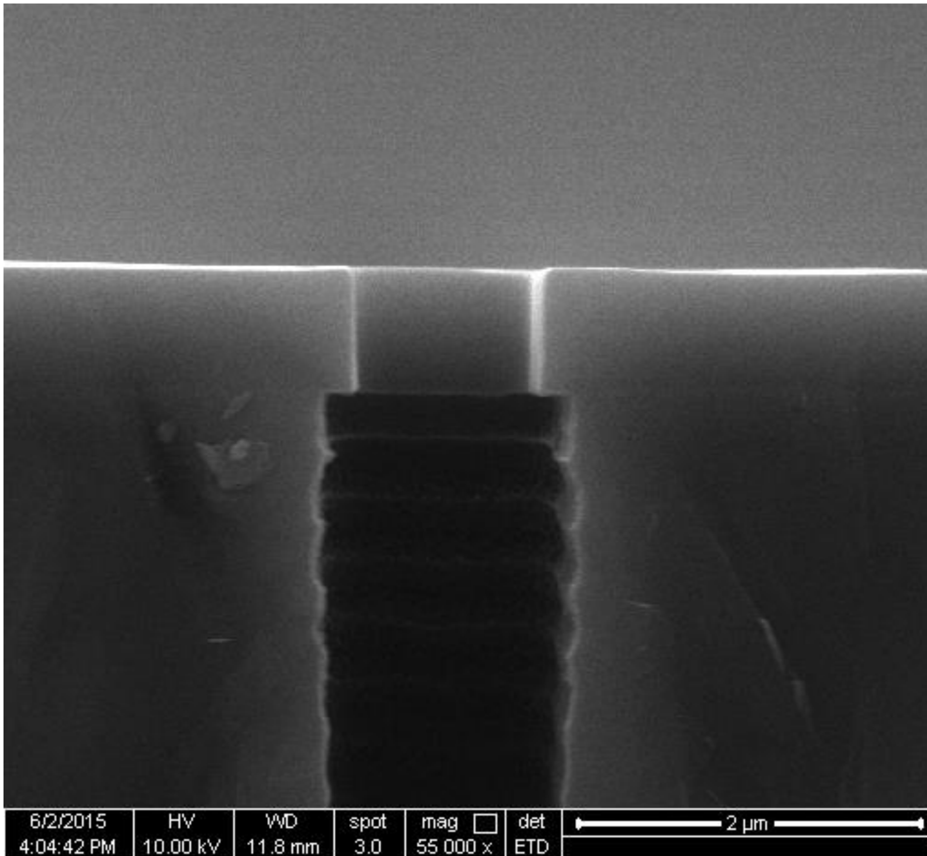

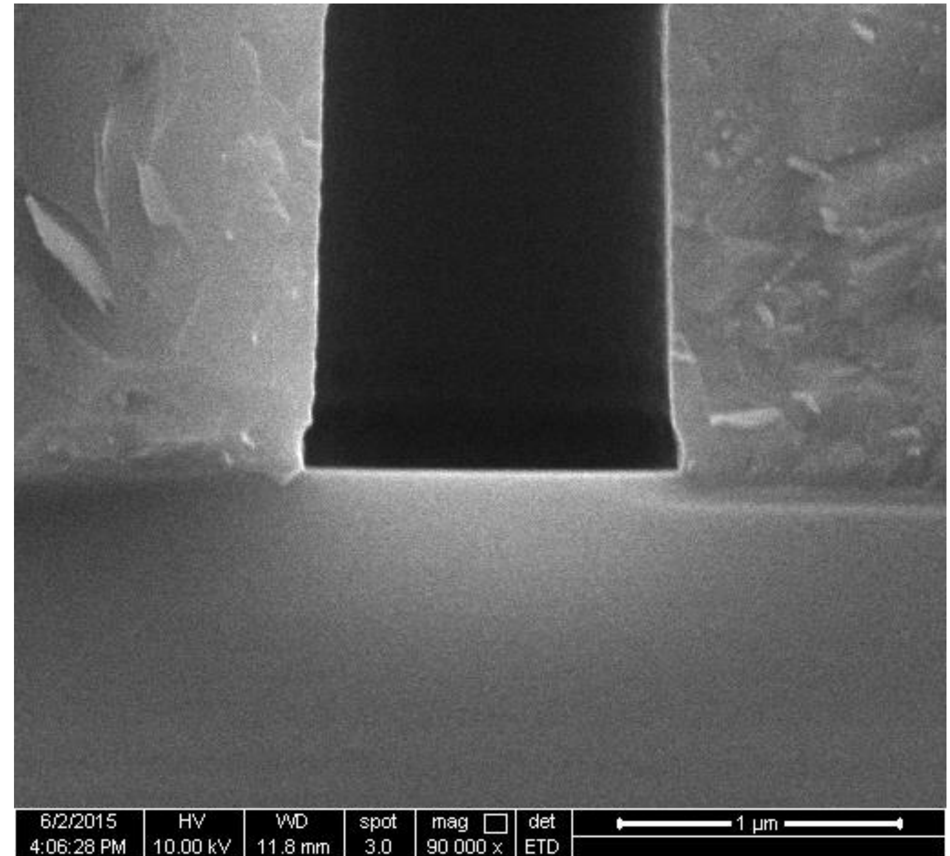

Contributions

- Variable trench optimization (0.7 – 1.5 um widths)
  - 20um
  - 40um
- PT-DSE has waveform pulsing issues
  - Manufacturer level issue
  - SOI development may be continued upon resolution
    - Optimized recipes may be used for HAR variable trenches

Thanks! & Questions?