Block Copolymer Etching for Hole Shrink Applications

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ENGR 241 – Winter 2019

Introduction:

For patterning at the 5 nm node and beyond, resolving the increasingly tight pitch requirements of integrated circuits (ICs) is hugely challenging. Currently, multiple patterning with 193 nm immersion lithography is in production [1], but the cost and complexity of multiple patterning is increasingly untenable as more patterning steps are required for next-generation ICs [2]. Due to recent improvements in the source power and throughput of extreme ultraviolet (EUV) lithography tools, EUV is expected to be in production for the 7 nm node [3]. However, it is already anticipated that EUV double-patterning will be necessary within a couple generations [4] and that the patterning costs per wafer will only continue to rise. Given this outlook, there is definite appetite for cost-saving lithography techniques. One promising solution is block copolymer (BCP) directed self-assembly (DSA), which produces high-resolution patterns at a low cost and high throughput. Block copolymers consist of two polymers covalently bonded end-to-end. One industry-standard [5] BCP is 70:30 PS-*b*-PMMA, in which a long PS chain is joined to a short PMMA chain, as illustrated in Figure 1-a. At room temperature, the PS and PMMA blocks will be randomly oriented in a PS-*b*-PMMA film. However, with adequate thermal energy, the BCPs will be driven to their minimum free-energy position, in which the PMMA will aggregate into cylinders surrounded by a PS matrix (see Figure 1-b). By selectively removing the PMMA cylinders, a PS soft mask with 20-nm holes can be obtained and used for further patterning.

On unpatterned substrates, this self-assembly process forms hexagonally packed holes with long-range order. For IC applications, however, this hexagonal hole placement is incongruous with the aperiodic layout of contacts and vias. As a result, it is necessary to confine the self-assembled features in guiding wells to enable arbitrary pattern placement. In this

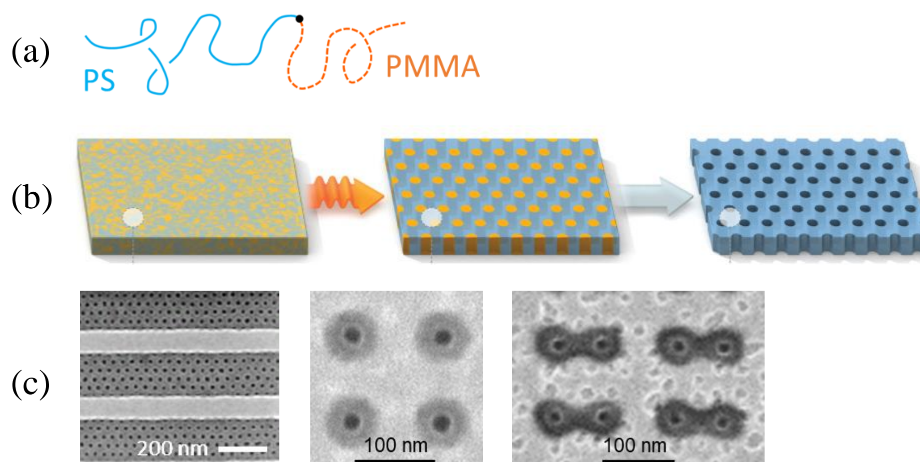


Figure 1: Illustration of the self-assembly process using (a) PS-*b*-PMMA. Unguided, a block copolymer film can self-assemble into (b) an array of hexagonally packed cylinders. Image credit (b): [6]. Guiding wells used in DSA confine (c) smaller clusters of cylinders. Image credit (c-left): [7]. The self-assembled cylinders can be removed and the pattern transferred into the substrate.

method, clusters of one or more self-assembled holes can be formed based on the size of the guiding wells, as shown in Figure 1-c. These wells not only direct the self-assembly process, but also act as a protective mask for the regions of the sample where no self-assembled patterns are wanted. Through clever sizing and positioning of the guiding wells, DSA holes can be placed into arbitrary layouts. While the industry interest in DSA is primary targeted at extended the resolution of multiple patterning [8] or EUV lithography [9], DSA can be used at the Stanford Nanofabrication Facility (SNF) to complement the i-line stepper (asml*) or the Raith 150 e-beam writer (raith).

* Underlined names in this report refer to equipment in SNF/ExFab or SNSF

Project Objective:

The goal of this project is to implement a DSA process at SNF that uses PS-*b*-PMMA to etch holes with critical dimensions (CDs) of 20 nm. In our previous reports [10, 11], we proposed the use of SiO_2/TiN guiding wells and demonstrated their fabrication. We have also detailed a DSA flow that can be fully carried out by labmembers in SNF and shown preliminary etch results of the BCP holes into the TiN hard mask. In this report, we will discuss further improvements to the guiding well etch and methods for characterizing the pattern transfer into the TiN. Because we ultimately intend to use this process to etch SiO_2, we also describe the results of using the etched TiN hard mask to transfer the DSA holes into SiO_2. The full process flow is illustrated in Figure 2.

Experimental Methods:

SiO_2 deposition: Silicon dioxide was deposited onto a bare Si wafer in ccp-dep, a plasma-enhanced chemical vapor deposition (PECVD) system. The built-in SiO350-0 recipe was used, the details of which shown in the Table 1. After a deposition time of 67 s, the thickness of the deposited SiO_2 layer was measured using spectro-reflectometry (nanospec) to be 70 nm.

SiO_2/TiN guiding well deposition: Titanium nitride (TiN) was sputtered (lesker-sputter) onto the SiO_2 layer using the deposition recipe in Table 2. We previously [10] measured the deposition rate to be 31.4 nm/hr, and based on this rate, we used a deposition of 30 min to deposit 15.7 nm of TiN. Next, a 100-nm SiO_2 layer was deposited (ccp-dep) onto the TiN using a deposition time of 98 s. The SiO_2 deposition followed the same recipe given in Table 1.

Guiding well patterning: Before patterning, the wafer was spin-coated with 950K PMMA A3 e-beam resist. We used a spin speed of 2000 rpm to achieve a PMMA thickness of ~150 nm. This resist layer was hard-baked for 90 s on a hot plate at 180 °C and exposed in the JEOL e-beam lithography tool in SNSF. After exposure, the wafer was developed in 1:3 MIBK:IPA for 30 s. The e-beam pattern contained 13.5 × 13.5 µm arrays of circles with diameters of 40 - 100 nm. To capture a wider range of guiding well sizes, a dose array was printed from 1000 $\mu C/cm^2$ to 2000 $\mu C/cm^2$ in 100 $\mu C/cm^2$ increments. The target guiding well CD to create a single-hole DSA pattern is ~80 nm [12].

Figure 2: Diagram of full process for SiO_2/TiN guiding well fabrication, directed self-assembly, and pattern transfer into TiN and SiO_2.

Table 1: TiN Sputtering Conditions

Target	TiN
Pressure	5 mTorr
Power	150 W
Ar Flow	10 sccm
N_2 Flow	20 sccm

Table 2: SiO_2 CVD Conditions

Pressure	1100 mTorr
Power	200 W
Temp	350 °C
SiH_4 Flow	250 sccm
He Flow	800 sccm
N_2O Flow	1700 sccm

Table 3: Guiding Well Etch Conditions and Rates

Pressure	30 mTorr
Power	200 W
CHF_3 Flow	20 sccm
CF_4 Flow	5 sccm
Ar Flow	10 sccm
PMMA Etch	27 nm/min
SiO_2 Etch	51 nm/min
TiN Etch	20 nm/min

Guiding well etch: The fabrication of the guiding wells in SiO_2 was completed in oxford-rie, a capacitively coupled plasma etcher, using the recipe given in Table 3. Different methods were used to measure the etch rates of the materials involved: the changes in thickness before and after etching for SiO_2 and PMMA were determined using nanospec, while the change in thickness for TiN had to be measured in a profilometer (Dektak Styler Profiler in SNSF) due to poor TiN model fitting in the ellipsometer (woollam). The measured etch rates for these materials are also given in Table 3. Due to RIE lag [13], an etch time of 162 s was necessary to completely etch through the SiO_2 layer. After etching, the excess PMMA resist was removed in the Drytek plasma etcher (drytek2) using the built-in descum recipe for 5 min. The descum recipe is given in Table 4.

Table 4: Descum Etch Conditions	
Pressure	150 mTorr
Power	500 W
Temp	350 °C
O_2 Flow	100 sccm

Block copolymer directed self-assembly: Outside of SNF, a 1 wt% BCP solution was mixed using a PS-*b*-PMMA block copolymer with M_w = 46.1-*b*-21.0 kg/mol, as purchased through Polymer Source, Inc. (P2400-SMMA). The solvent used was propylene glycol monomethyl ether acetate (PGMEA) purchased from Sigma-Aldrich. This solution was coated onto the samples after guiding well fabrication using the headway3 spin coater. The film was spun at 2500 rpm for 60 s. Next, the pieces were baked in white-oven at 200 °C for 10 min to enable the formation of PMMA cylinders by self-assembly. In order to break the covalent bonds in the PMMA blocks, the samples were exposed (intensity = 6mW/cm^2 at λ = 220 nm) to deep UV radiation (Oriel, SNF) for 3 s. The PMMA cylinders could then be developed away by soaking the samples in acetic acid for 10 min, leaving vacancies in the PS soft mask. Figures 3 and 4 show an illustration of the DSA process and a top-down SEM image (Magellan, SNSF) of the PS soft mask after PMMA removal, respectively.

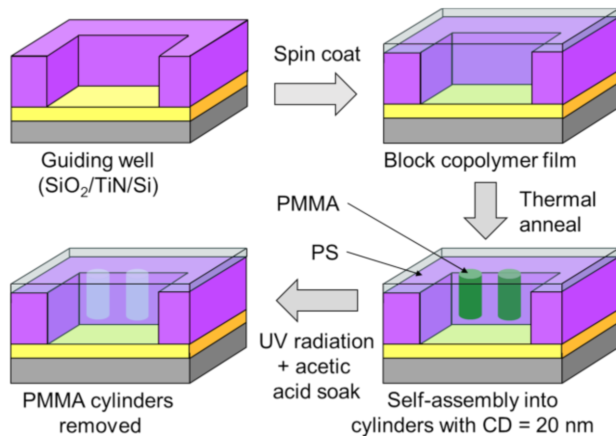


Figure 3: Drawing of DSA process for PS-*b*-PMMA in two-hole SiO_2/TiN guiding wells.

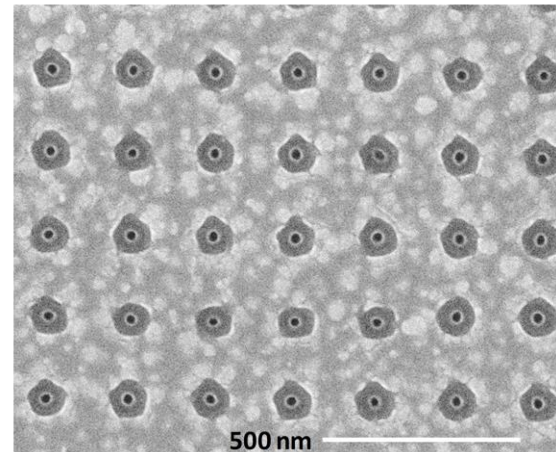


Figure 4: SEM image of the DSA holes after PMMA removal.

TiN hard mask etch: The PlasmaTherm inductively coupled plama (ICP) metal etcher (pt-mtl) was used to transfer the pattern from the PS soft mask into the TiN hard mask. This etch consisted of two steps: first, etching through the residual PS layer at the bottom of the guiding well and second, transferring the hole in into TiN. The etch rate of TiN was previously [10] measured to be 17.9 nm/min using the TiN etch recipe given in Table 5. To fully etch through

Table 5: TiN Etch Conditions	
Pressure	10 mTorr
Bias Power	50 W
Cl_2 Flow	30 sccm
BCl_3 Flow	5 sccm
Ar Flow	10 sccm

the TiN layer, an etch time of 100 s was used. Afterwards, the remaining PS soft mask was removed in drytek2 using the descum recipe in Table 4 for 5 min.

Si decoration etch: The Si etch was completed in another PlasmaTherm ICP etcher (pt-dse) that uses the Bosch process to etch high aspect ratio features in Si using alternating cycles of SF_6 and C_4F_8. In the SF_6 cycles, the Si is etched. During the C_4F_8 cycles, the newly-exposed Si surface will be protected by polymer deposited. These cycles work together to prevent the sidewalls from being etched while etching deeper into the substrate [14]. To decorate the TiN holes, the built-in nano recipe was used for 20 cycles to transfer the DSA holes from the TiN into the Si wafer.

Pattern transfer into SiO_2: This step uses the same recipe as the guiding well etch, as given in Table 2. We have not so far been able to determine the maximum etch time, which is limited by the etch rate of the TiN hard mask. Based on our experiments, which we will discuss below, we obtained partial SiO_2 etches for etch times of 30 s and 50 s. We also discovered that an etch time of 120 s was too long.

Results and Discussion:

Improvements to the guiding well etch: Ideally, the guiding well should be a cylindrical hole with vertical sidewalls. The height of the cylinder should be the same as the thickness of SiO_2, leaving the TiN layer underneath exposed. In reality, the guiding well shape will differ from the theoretical case. First, the sidewalls may not be perpendicular to the bottom of the well. The PS soft mask tends to follow the sidewall angle of the guiding well, so vertical sidewalls are important to maintaining vertical sidewalls in the resulting PS soft mask. Second, the depth of the guiding well etch, as determined by the etch time, can greatly affect the pattern transfer results. Insufficient guiding well etch time will lead to residual SiO_2 at the bottom of the well. Any SiO_2 left there will impede the pattern transfer from the PS soft mask into the TiN hard mask layer, as the gases used etch the TiN will not etch SiO_2 well. In comparison, excessive guiding well etch time will guarantee exposure of the TiN but will also damage the already thin layer, making it less able to able to function as a hard mask. Thus, our goal is to find an etch time that will clear all the SiO_2 from the wells without overetching the TiN.

Table 6: Comparison of Guiding Well Etch Conditions			
	Recipe 1	Recipe 2	Recipe 3
Power	100 W	200 W	200 W
Pressure	30 mTorr	40 mTorr	30 mTorr
Flow [sccm]	20 CHF_3 / 5 CF_4 / 10 Ar	25 CHF_3 / 10 Ar	20 CHF_3 / 5 CF_4 / 10 Ar
Bias Voltage	407 V	518 V	525 V
PMMA Etch	16 nm/min	11 nm/min	27 nm/min
SiO_2 Etch	27 nm/min	51 nm/min	51 nm/min
TiN Etch	20 nm/min	16 nm/min	20 nm/min

Table 6 shows the guiding well etch recipe from our previous [11] report (Recipe 1) and an etch recipe modified to improve selectivity (Recipe 2) by changing the power and pressure, and gas flows. The etch rates for these materials were measured using the same methods discussed earlier and are also given in Table 6. Here, we see that the modifications in Recipe 2 nearly double the SiO_2 etch rate, while decreasing the etch rates of PMMA and TiN. However, when the guiding wells etched with Recipe 2 were imaged in cross-section (see Figure 5), the sidewall angle of the guiding wells appears appear to have become very slanted. For this reason, we did not pursue this recipe further.

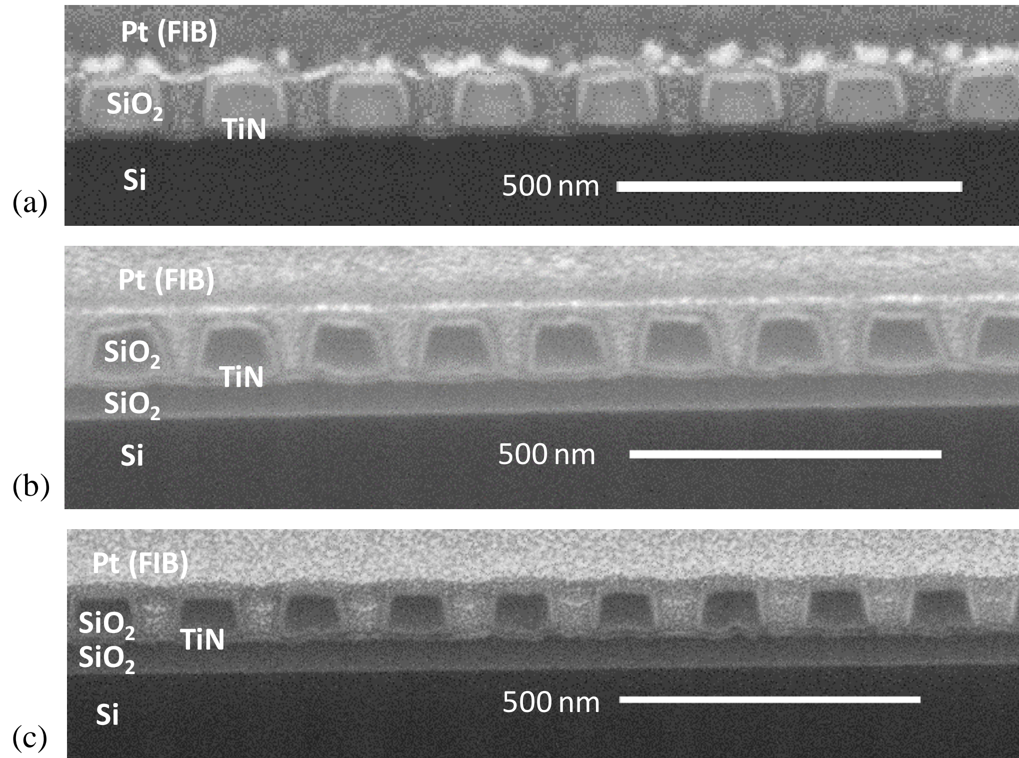
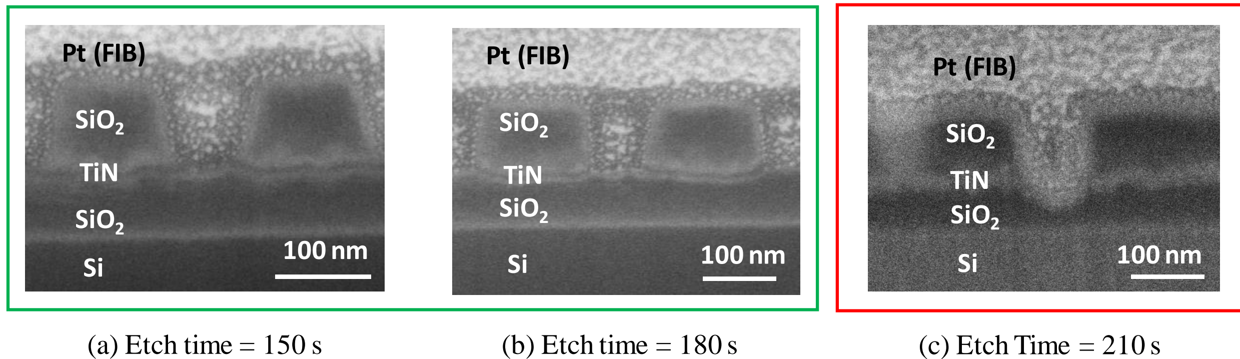


Figure 5: Cross-sectional images (Helios, SNSF) of the guiding well etched using (a) using Recipe 1, (b) Recipe 2, and (c) Recipe 3. In (b), the sidewalls are noticeably slanted compared to the more vertical sidewalls in (a) and (c).



(a) Etch time = 150 s (b) Etch time = 180 s (c) Etch Time = 210 s

Figure 6: Cross-sectional images (Helios, SNSF) of the guiding wells etched with Recipe 3 for etch times of (a) 150 s, (b) 180 s, and (c) 210 s. Here, we see that the etches in (a) and (b) have etched through the SiO_2 film without significant overetch, whereas the etch in (c) has cut into the underlying SiO_2 layer.

Keeping the same chemistry as used in Recipe 1, Recipe 3 only adjusts the bias power to preserve vertical sidewall angle (see Figure 5-c). The guiding wells were etched with Recipe 3 for different lengths of time (150 s, 180 s, and 210 s) to find the right etch time. As shown in Figure 6, the samples etched for 150 s and 180 s both appeared to be within the process window, but the sample etched for 210 s was very overetched. To be in the middle of the process window, we decided on 162 s as a good choice for opening the guiding wells in SiO_2.

Characterization of pattern transfer into TiN: Following the guiding well fabrication and subsequent DSA process, the self-assembled holes from the PS soft mask are transferred into the underlying TiN hard mask. Next, the holes should be further transferred into the underlying SiO_2 layer, but it is critical to first characterize the holes etched in the TiN film. Without understanding the size and shape of the TiN holes, troubleshooting any problems that arise in the next pattern transfer step becomes extremely challenging. However, it quickly became apparent that characterizing the TiN holes was a non-trivial task. To start with, the etched features are challenging to observe because of their small size and depth. To add complexity, the numerous uncertainties in the DSA process, especially with regards to the profile of the PS soft mask, make it difficult to deconvolve process failures and characterization failures. That is, if a given characterization technique yields no evidence of pattern transfer, it is not easy to decipher whether there was no pattern to observe in the first place (i.e. process failure) or if we missed the pattern that was there (i.e. characterization failure). Here, we will describe some of the methods that we used to characterize the TiN holes and the degree to which they were successful.

When confronted with a characterization problem, the first question is what tool to use. Given the small size of the TiN holes, we narrowed down the possibilities to the scanning electron microscope (SEM) and focused ion beam (FIB). While transmission electron microscopy (TEM) would also be a reasonable candidate, the long preparation time and low throughput of making and imaging TEM samples made this option unattractive. Atomic force microscopy (AFM) was also not considered due to the need for prohibitively expensive high aspect ratio tips.

In our previous report, we described the result of imaging the SiO_2/TiN stack in SEM [11]. With the relatively low aspect ratio (< 1.5:1) of the guiding well and long mean-free path of the electrons in the vacuum chamber (< 10^{-4} mbar), imaging the TiN at the base of the well should technically be possible. However, as illustrated in Figure 7, the bright edges of the SiO_2 guiding wells obscure any features at the base of the well and make it difficult to ascertain what, if any, pattern has been transferred into the TiN.

Next, we used FIB to access the cross-section of the TiN holes. The protective Pt coating deposited in the FIB onto the sample before ion milling helps to mitigate the charging effects along the edges of the SiO_2. Figure 8 shows a cross-sectional image of the etched TiN film sandwiched between the two SiO_2 layers. Unlike the SiO_2/Pt interface, the TiN/Pt interface in this image lacks contrast, making it difficult to pinpoint the position of the TiN edge. Furthermore, the underlying SiO_2 layer is so rough and the TiN film is so thin that the profile of the base of the guiding wells cannot be easily interpreted. While the roughness of the guiding well base could be due to pattern transfer from the BCP soft mask, it could also be due to the roughness in the SiO_2 film. Given the failure of SEM and FIB to provide clear and unambiguous information about the TiN etch profile, we instead explored ways to make the etched features in the TiN film more obvious.

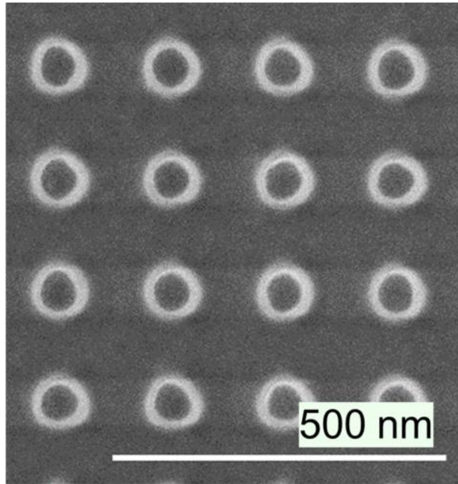


Figure 7: Top-down SEM image (Magellan, SNSF) of the guiding wells after pattern transfer into the TiN and removal of the PS soft mask. The bright edges of the guiding wells obscure the interior of the wells.

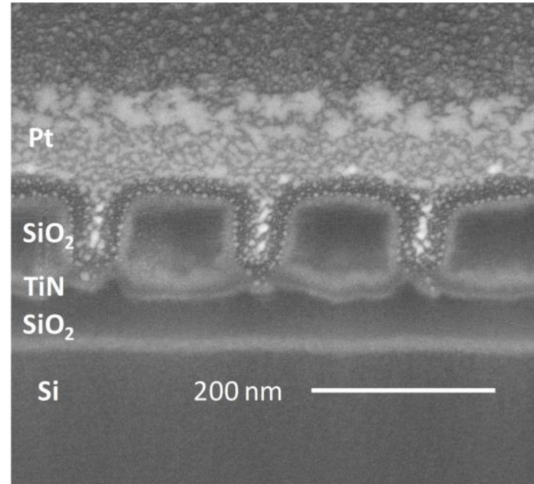


Figure 8: Cross-sectional image (Helios, SNSF) of the guiding wells after pattern transfer into the TiN and removal of the PS soft mask. The profile of the bottom of the guiding wells are not easily interpreted.

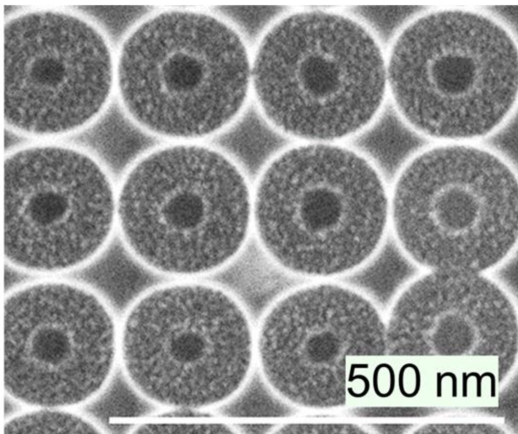


Figure 9: Top-down SEM image (Magellan, SNSF) of the guiding wells after pattern transfer into the TiN and a 60 s etch in 20:1 BOE. The bright rings outline the remaining SiO_2, and the smaller dark circles are the enlarged holes in the TiN hard mask.

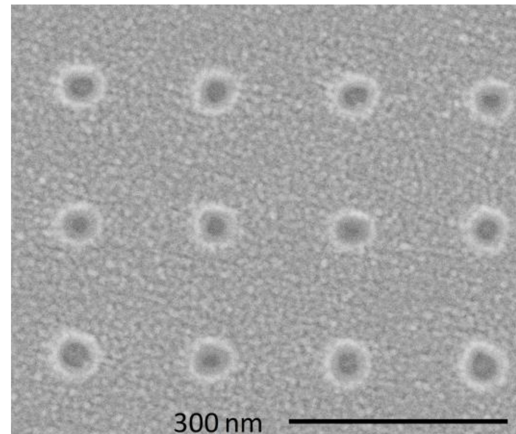


Figure 10: Top-down SEM image (Magellan, SNSF) of the guiding wells after pattern transfer into the TiN and a 90 s etch in 20:1 BOE. The bright rings outline the further enlarged TiN openings, and the smaller dark circles are the overetched holes in the Si substrate.

The seemingly most straightforward of these approaches would be to remove the SiO_2 layer in order to make the TiN hard mask more visible. Unfortunately, we could not find a method of etching the SiO_2 without also etching the TiN film, especially since the TiN was oxidized from the O_2 plasma clean used to remove the e-beam resist after the guiding well etch. Previously [11], we reported the results of soaking the sample after a TiN etch of 70 s in 20:1 BOE for 60 s to partially removed the SiO_2. With the SiO_2 etched back significantly, we were able the confirm that there was some degree of pattern transfer into the TiN (see Figure 9). However, because the BOE enlarged the TiN holes, we were unable to gather additional relevant information about the pattern transfer beyond the fact that it existed.

Because removing the SiO_2 guiding layer from the TiN film was not a viable solution, we indirectly characterized the TiN etch by overetching into the Si substrate. Images of the overetch can indirectly provide information about the CD of the TiN holes through the CD of the overetched Si holes. Visible overetch into the Si also implies that the depth of the TiN etch was enough to etch through the whole film. To highlight the overetch, the TiN etch was extended from 70 s to 100 s to deepen the features, and the 20:1 BOE soak was extended from 60 s to 90 s. As shown in Figure 10, the extra time in BOE completely stripped the SiO_2 and further enlarged the TiN holes. In the middle of the TiN openings, overetch into the Si is visible, indicating that an etch time of 100 s is enough to etch through the TiN film. The CDs of the overetched holes are 20-30 nm, which is as expected for the BCP used in this study.

To confirm that the smaller features inside the TiN openings were indeed overetched holes, the TiN was stripped from the Si in a 9:1 piranha soak for 20 min. Small holes can still be observed in the Si surface, confirming that they have been etched into the Si (see Figure 11-a). Although the CDs of these features appear to be in the same range as the CDs measured in sample with the TiN film, the images are so blurry that it is difficult to obtain precise measurements. Notably, even for long dwell times, the features etched into the Si were practically invisible in the SEM, making it extremely difficult to focus and stigmate the beam properly. While not the primary cause, we suspected that oxide on the Si surface was contributing to the poor feature visibility. Piranha is strongly oxidizing and will form a thin chemical oxide on Si. In this case, the oxide was measured to be 4.3 nm thick via ellipsometry (woollam) and was then stripped in 20:1 BOE for 30 s. Following the oxide removal, the features were marginally easier to see, allowing us to obtain slightly sharper SEM images (see Figure 11-b). While these images corroborate our hypothesis that the small features we observed inside the TiN holes in Figure 10 result from overetch, they still lack the sharpness that we found in the images with the TiN film, as facilitated by the visible grains in the TiN film.

Based on the presence of visible overetch, we know that the TiN film has been completely etched through. However, it is important not to overetch the film unnecessarily to preserve the integrity of the thin hard mask. In order to ascertain the minimum time needed to etch through the TiN hard mask, shorter TiN etch times need to be characterized. However, at

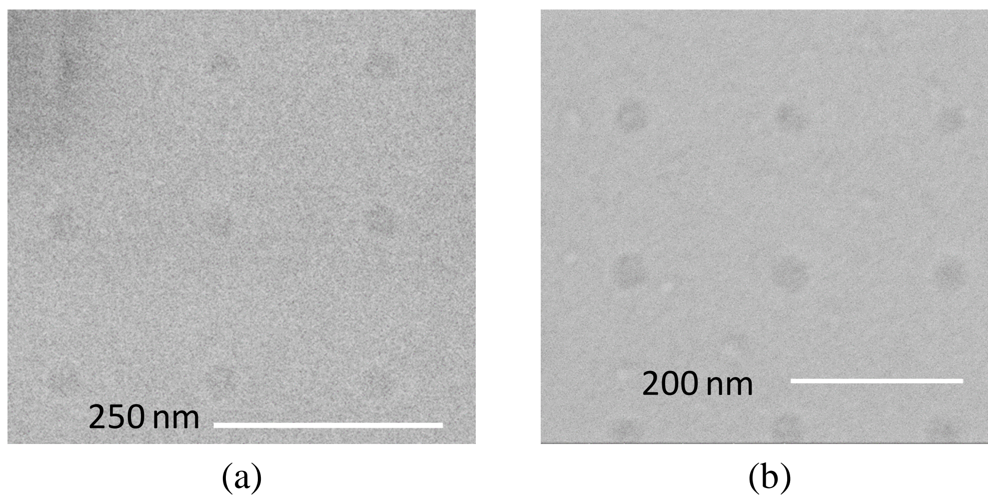


Figure 11: Top-down SEM images (Magellan, SNSF) of overetch of the TiN film into Si (a) before and (b) after the oxide grown by piranha was cleaned from the surface. Although the image is slightly sharper in (b), neither image provides clear indication of where the edges of the Si holes are.

these shorter etch times, imaging the overetch will present an even greater challenge. In SEM, edges generally appear bright, as they have more surface area from which low-energy secondary electrons can escape [15]. Already, the Si holes are very shallow and therefore lack the same bright edge effect that sharply defines the edges of deeper features. As the overetch becomes increasingly shallow, the edges of the Si holes will become increasingly poorly defined. For this reason, it is necessary to find ways to transfer the patterns deeper into the Si as a means of decorating the TiN holes.

Si decoration etch: At first, we thought to decorate the TiN holes using XeF_2 (xactix), a vapor that isotropically etches Si. This technique is used to highlight pinholes in atomic layer deposition (ALD) films [16], as the XeF_2 will etch the Si underneath the pinholes. Due to the isotropic nature of the etch, the enlarged holes in Si are much easier to find than the original ALD pinholes. While XeF_2 was initially promising for highlighting through holes in the TiN, we found that it was overly aggressive. Moreover, the XeF_2 also etched the TiN, making it ambiguous whether the Si was etched due to through holes in the TiN from the BCP soft mask pattern transfer or due to XeF_2-created through holes in the TiN film that were not previously there. In the end, we did not find the XeF_2 to give clear results on whether the Si was exposed.

Looking at other methods of transferring the TiN hole deeper into the Si, we targeted anisotropic etches in order to maintain the CD of the TiN hole during the Si etch. This led us to the Bosch process (pt-dse). Because of the sidewall passivation steps, the CD of the TiN holes can be better maintained during the Si etch. Figure 12 shows the sample after 20 etch cycles and full TiN removal for increasing guiding well sizes. For undersized guiding wells, the block copolymer will not produce a deep PMMA vacancy, so there should be no pattern transfer into the TiN and Si [12]. The increasing hole-open yield for increasing guiding well CD makes sense in that light. Notably, the DSA hole size should not change significantly based on guiding well size, and indeed, our measurements indicate that the average size of the Si holes does not have any clear trend with changes in guiding well size. Based on the previously measured DSA hole

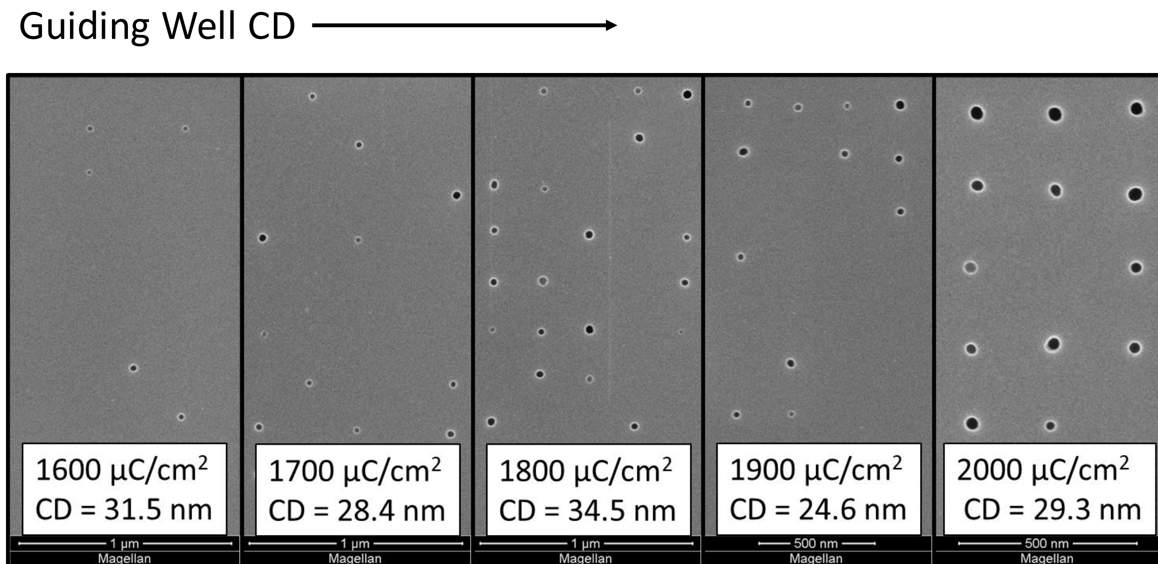


Figure 12: Top-down SEM images (Magellan, SNSF) of the holes transferred into the Si substrate from the TiN hard mask. The TiN has been removed to leave bare Si. As the dose of the e-beam is increased, the guiding well CD also increases. We see that for larger guiding well CD, more holes are seen in the Si.

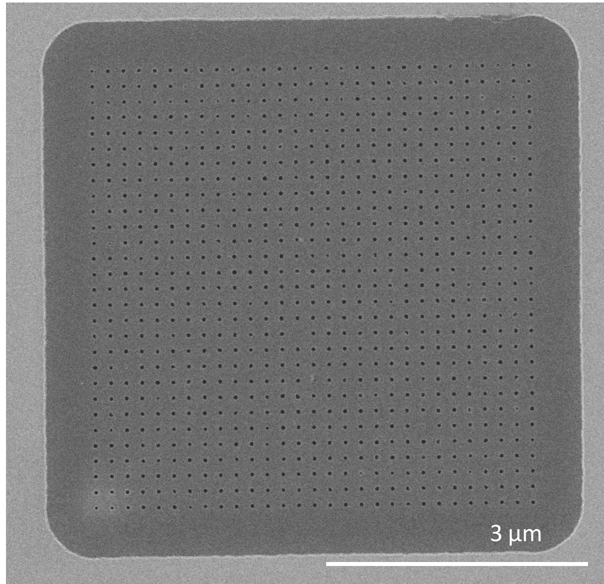


Figure 13: Top-down SEM images (Magellan, SNSF) after TiN removal of the pattern transferred into the Si substrate from the TiN hard mask. The dark square surrounding the smaller holes indicate the TiN did not effectively mask the Si surface.

sizes, the CDs of the Si holes (20 - 30 nm) are in line with expectations. These results indicate successful DSA pattern transfer into TiN and Si and validate our general process flow.

While this initial pattern transfer demonstration shows promise, we have so far struggled to replicate the results. Even for pieces from the same wafer as the successful sample, the Bosch process etching yields significantly different results. Figure 13 reveals small holes in the Si set inside a larger etched box, the size of which resembles the size of the guiding well array. Here, the Si holes average CD $\approx$ 45 nm, which is larger than expected based on the measurements from the previous sample. More importantly, the etching of the entire guiding well array area indicates that the TiN has not effectively masked the Si and suggests that the TiN film was likely thinned significantly during one or more of the etches. This inability to replicate the pattern transfer points to significant variation in the guiding well fabrication, DSA process, pattern transfer, or a combination of these. Further testing and more frequent characterization are necessary to diagnose the source of the variation.

In the meantime, we have been unable to carry out our initial plan to use the Bosch process decoration to check the progress of the TiN etch. Even so, both the sample with observed Si overetch and the sample with successful Bosch process decoration used an etch time of 100 s to transfer the pattern from the BCP soft mask into the TiN. In both cases, this etch time was enough to etch all the way through the TiN film. Although a shorter TiN etch time could likely be used, we can proceed cautiously with the 100 s TiN etch and check the intermediate steps of the process more carefully to monitor process variation.

Pattern transfer into the SiO_2 underlayer: Although transferring the BCP holes into Si is useful as a characterization step, the goal of our project is ultimately to use DSA to etch SiO_2. Based on our TiN etch characterization results, we moved forward with executing the guiding well fabrication, DSA process, and TiN etch on pieces from a wafer with an underlying SiO_2 layer. After the TiN etch, the pattern was transferred from the TiN into the SiO_2 underneath. Figure 14 shows resulting etch profile for etch times of 30 s, 50 s, and 120 s. In these images, we can see the SiO_2 is etched to varying depths. Even for the shortest etch time (t = 30 s), though, no hole shrink is observed. Instead, it looks as though the guiding well size was directly etched into the bottom SiO_2 layer.

In an effort to protect the TiN and enable further etch depth, the BCP soft mask was not removed from these samples after the TiN etch and before the SiO_2 etch. However, soft masks are typically removed after the hard mask etch due to redeposition issues. For this reason, we tried the experiment again, adding the step of removing the BCP after the TiN etch. The BCP

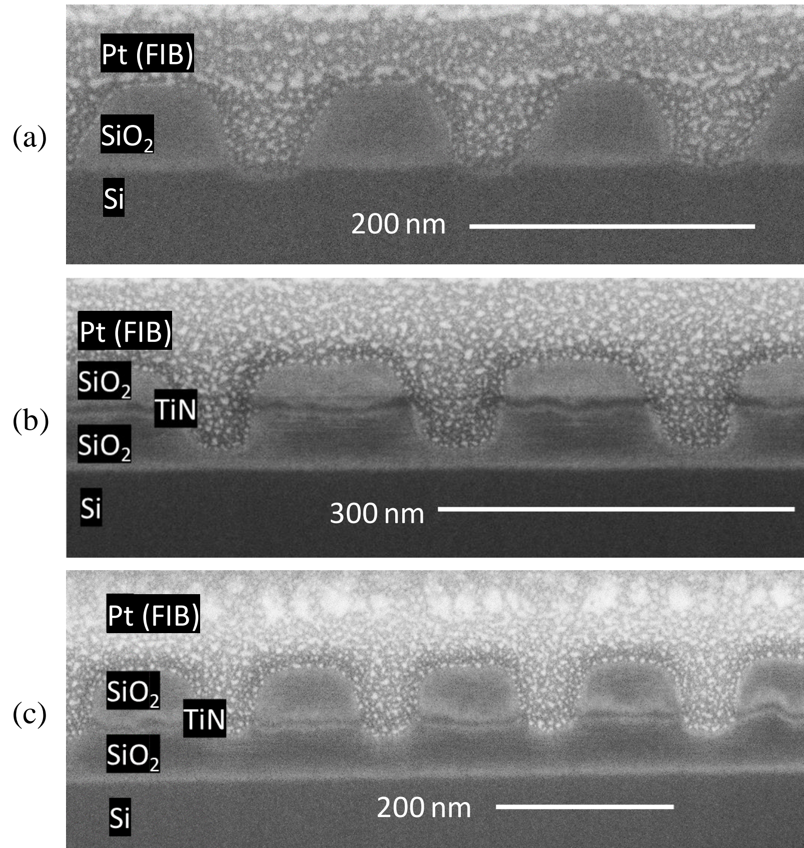


Figure 14: Cross-sectional FIB images (Helios, SNSF) of the pattern transfer from the TiN hard mask into the underlying SiO_2 without first removing the PS soft mask. The samples were etched for (a) 120 s, (b) 50 s, and (c) 30 s. While etch into the SiO_2 is visible, none of the images show hole shrink.

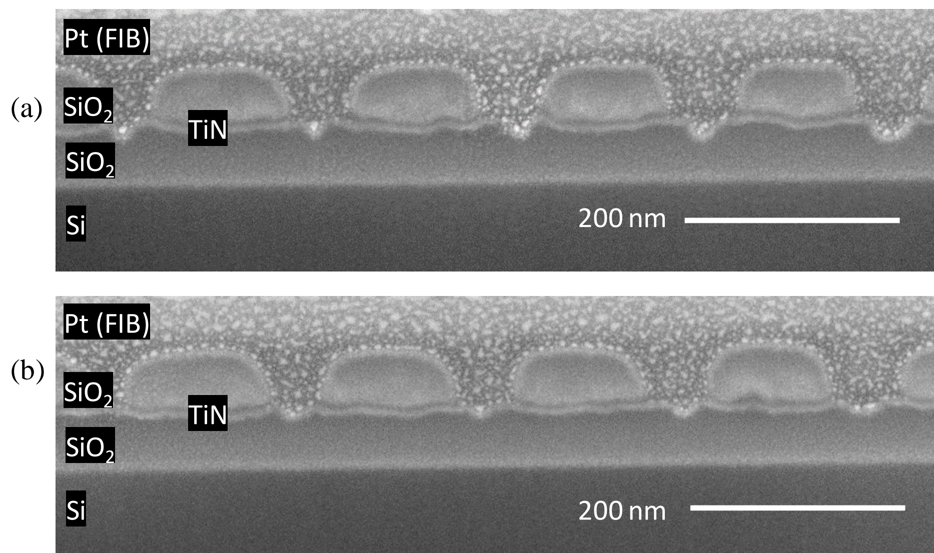


Figure 15: Cross-sectional FIB images (Helios, SNSF) of the pattern transfer from the TiN hard mask into the underlying SiO_2 after removing the PS soft mask. The samples were etched for (a) 50 s and (b) 30 s. In both cases, successful hole shrink is can be seen.

was removed using an O_2 plasma descum etch. Figure 15 shows the cross-section of the etched features in the underlying SiO_2. Here, we see shallow holes in the SiO_2 surface that are of a reduced CD relative to the guiding well size. Indeed, these images appear to confirm successful pattern transfer of BCP soft mask pattern into the SiO_2. The SiO_2 holes have CD of 15-30 nm and a depth of < 20 nm. Notably, the patterns are shallow and need to be much deeper in order to be practically useful for device fabrication. There does not appear to be anything left of the TiN hard masks after these etches to enable deeper pattern transfer, but as noted earlier in this paper, the TiN layer has proven difficult to clearly see in cross-section. Further tests are needed to verify whether a deeper etch can be achieved with the TiN hard mask, but these initial etch results show a good deal of promise.

Conclusion:

In this report, we discuss transferring 20-nm block copolymer holes into a TiN hard mask and ultimately into SiO_2. Because the thickness of the TiN hard mask is so critical to enabling the pattern transfer, we adjusted the SiO_2 guiding well etch recipe to achieve greater selectivity between the SiO_2 and TiN. Although the etch chemistry remained the same, the increase in bias power raised the SiO_2 etch rate, while keeping the TiN etch rate nearly the same. With the improved selectivity, we were able to ensure that the SiO_2 guiding wells were etched through without unnecessarily thinning the TiN hard mask. Next, we explored many options for characterizing the TiN etch. Because direct inspection of the sample was found to have limited utility, we shifted our focus to decorating the TiN etch by modifying the Si substrate. Despite challenges with process variation, we achieved reasonable results with transferring the TiN holes into Si using the Bosch process. From the Si etch results, we were able to show that the BCP pattern was successfully transferred into the TiN layer. Finally, we were able to demonstrate successful pattern transfer from the TiN hard mask into the underlying SiO_2 layer. While the final etched patterns in SiO_2 were shallow, they had the desired CD ≈ 20 nm, indicating successful hole shrink. Looking ahead, our next step is to etch the holes even deeper. The current hard mask may not be able to withstand a deeper etch, so we plan to try a thicker TiN hard mask or to choose another hard mask material with better etch selectivity to SiO_2. Nevertheless, these initial etch results suggest that the current process flow has potential and with some adjustments, we hope to etch deep enough features to integrate DSA into device fabrication processes at SNF.

References:

[1] R. Courtland, “The Status of Moore’s Law: It’s Complicated,” *IEEE Spectr.*, Oct. 2013.
[2] Y. Chen, Q. Cheng, and W. Kang, “Technological merits, process complexity, and cost analysis of self-aligned multiple patterning,” in *Proc. SPIE*, vol. 8326, no. 832620, 2012.
[3] S. K. Moore, “EUV Lithography Finally Ready for Chip Manufacturing,” *IEEE Spectr.*, Jan. 2018.
[4] R.-H. R. Kim, “EUV insertion strategy into logic technology on the horizon of scaling paradigm change,” presented at SPIE Adv. Lith., San Jose, CA, 2019.
[5] R. Ruiz *et al.*, “Density Multiplication and Improved Lithography by Directed Block Copolymer Assembly,” *Science*, vol. 321, no. 5891, pp. 936-939, 2008.
[6] R. Courtland, “Self-Assembly Takes Shape,” *IEEE Spectrum*, Jan. 2012.
[7] L.-W. Chang, “Device/Circuit Fabrication using Diblock Copolymer Lithography,” Ph.D. dissertation, Dept. Elect. Eng., Stanford Univ., Stanford, CA, 2010.
[8] I. Karageorgos *et al.*, “Design Strategy for Integrating DSA Via Patterning in sub-7 nm Interconnects,” in *Proc. SPIE*, vol. 9781, no. 97810N, 2016.
[9] R. Gronheid *et al.*, “EUV patterned templates with grapho-epitaxy DSA at the N5/N7 logic nodes,” in *Proc. SPIE*, vol. 9776, no. 97761W, 2016.
[10] M. C. Tung, “Enabling Pattern Transfer for Block Copolymer Directed Self-Assembly,” Stanford Univ., Stanford, CA, USA, June 2018. [Online]. Available: https://snfexfab.stanford.edu/process-summary/fab-project-courses-e241-ee412.
[11] M. C. Tung and H. Qiao, “Etching Block Copolymer Directed Self-Assembly Holes,” Stanford Univ., Stanford, CA, USA, Dec. 2018. [Online]. Available: https://snfexfab.stanford.edu/process-summary/fab-project-courses-e241-ee412.
[12] A. Latypov and T. H. Coskun, “Improving the lithographic process window using directed self-assembly-aware printing assist features,” *J. Micro/Nanolith. MEMS MOEMS*, vol. 14, no. 3, 2015.
[13] S. L. Lai, D. Johnson, and R. Westerman, “Aspect ratio dependent etching lag reduction in deep silicon etch processes,” *J. Vac. Sci. Technol. A*, vol. 24, no. 4, pp. 1283-1288, 2006.
[14] C. Chane *et al.*, “Etching submicrometer trenches by using the Bosch process and its applications to the fabrication of antireflection structures,” *J. Micomech. Microeng.*, vol. 15, no. 3, pp. 580-585, 2005.
[15] H. Seiler, “Secondary electron emission in the scanning electron microscope,” *J. Appl. Phys.*, vol. 54, no. 11, pp. R1-R18, 1983.
[16] M. Winterkorn, A. Dadlani, and Y. Kim, “Surface Micromachining Method for Releasing a Range of Micron-Scale Membranes,” Stanford Univ., Stanford, CA, USA, Dec. 2014. [Online]. Available: https://snfexfab.stanford.edu/process-summary/fab-project-courses-e241-ee412.