P-GaN/AlGAN/GaN E-mode HEMT

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1 Members of the Project

Anand Lalwani and **Seungbin Jeong** are the main students that comprise the team. We are both Ph.D. students in EE department at Stanford. Seungbin Jeong is a student of Stanford X-Lab lead by Prof. Debbie Senesky of AA department. Anand Lalwani is rotating in the group.

This team is mentored by SNF(Stanford Nanofabrication Facility) staff **Dr. Xiaoqing Xu**, as well as **Dr. Caitlin Chapin**, a post-doc researcher of the X-Lab. Also, external mentors **Dr. Donald Gardner** and **Dr. Dong Lee** kindly agreed to offer help and advice.

Position	Name
Student	Seungbin Jeong
Student	Anand Lalwani
SNF Staff	Xiaoqing Xu
Group Mentor	Caitlin Chapin
External Mentor	Donald Gardner
External Mentor	Dong Lee

Table 1: Participants of this project

2 Introduction

2.1 Wide Bandgap Semiconductors

We can start by talking about the **wide-bandgap(WBG)** semiconductor materials for readers not familiar with the concept. By wide-bandgap semiconductors, we refer to materials such as SiC, GaN whose bandgaps are typically above 3 eV. Conventionally many of them were regarded as insulators rather than semiconductors, but some of their superior properties as summarized in table 2 attracted many people and convinced them to use them as electronic materials. Their bandgap values lying in the range of 3 eV to 5 eV allow many optoelectronic devices. As these materials have higher breakdown field values, they can be widely used in the power electronics field. Moreover, their high electron mobility values combined with undoped channel techniques such as modulation doping results in high-performance transistors. Another extremely important property of those materials is that they are very thermally stable compared to conventional semiconductor materials, which makes them a very good choice for harsh environment electronics(e.g. space missions).

Property	Application
Wide Bandgap	Optoelectronics
High Breakdown Field	Power Electronics
High Electron Saturation Velocity	High Frequency Electronics
Thermal Stability	High Temperature Electronics

Table 2: Benefits of Wide-bandgap Materials

2.2 Gallium Nitride and 2DEG

Amongst various wide-bandgap materials that show good promises, this project is mainly about **GaN(gallium nitride)**. GaN-based heterostructures are frequently employed in high-frequency, high-power, and optoelectronic devices due to their wide bandgap, high breakdown voltage, high electron saturation velocity, and high thermal conductivity[1], just as mentioned above. Furthermore, GaN devices have demonstrated thermal stability up to 1000 °C in a vacuum, making GaN-based devices of great interest to the high-temperature device community and enabling their use in extreme environment applications where traditional semiconductor materials like Si cannot survive, such as Venus exploration[2]. However, what makes this particular material especially interesting is the heterostructure of gallium nitride and **aluminum gallium nitride($\mathbf{Al_xGa_{1-x}N}$)** , as in Fig.1a. As $Al_xGa_{1-x}N$ and GaN naturally have different lattice constants, there arises a tensile strain at the interface which causes a **piezoelectric polarization**, which adds to the **spontaneous polarazation** of the material[1]. The piezoelectric, spontaneous and total polarizations can be modeled as

$$P_{pz}(x) = (-6x + 9x^2)\ \mu\text{C} \cdot \text{cm}^{-2} \tag{1}$$

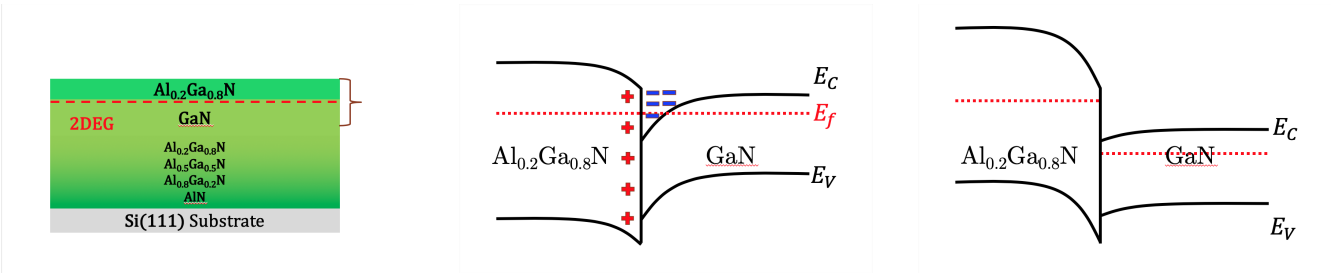
$$P_{sp}(x) = -10x\ \mu\text{C} \cdot \text{cm}^{-2} \tag{2}$$

$$P_{tot}(x) = P_{pz}(x) + P_{sp}(x) = -16x + 9x^2\ \mu\text{C} \cdot \text{cm}^{-2} \tag{3}$$

This polarization causes a net positive charge at the AlGaN/GaN interface, which in turn results in an electron accumulation right underneath it to compensate for this. We refer to this thin quantum well of electrons as in Fig.1a and Fig.1b as **2DEG(2-dimensional electron gas)**.

2.3 AlGaN/GaN HEMT and Depletion-mode Devices

Since the high density of AlGaN/GaN 2DEG carriers is not caused by doping, this AlGaN-GaN heterostructure allows us to take advantage of GaN's fast electron mobility as much as possible. Without ionized impurity scattering,



(a) AlGaN/GaN Structure on Si(111) Wafer with Graded $Al_xGa_{1-x}N$ Buffer

(b) Band Diagram of AlGaN/GaN Heterostructure with Zero Bias

(c) Band Diagram of AlGaN/GaN Heterostructure with Negative Bias

Figure 1: AlGaN/GaN Heterostructure

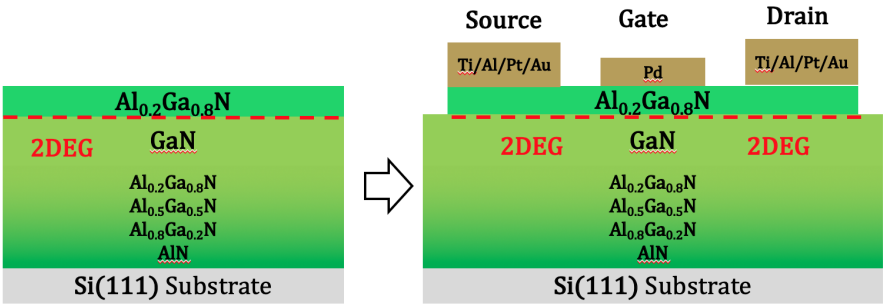


Figure 2: AlGaN/GaN HEMT Structure

we can expect the electron mobility of about $2000\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. Therefore transistors using these structures like Fig.2 are called **HEMT(high electron mobility transistor)**s.

However, this HEMT devices are depletion-mode devices due to the nature of the AlGaN/GaN heterostructure. **Depletion-mode devices** or **normally-on devices** are the devices that are turned-on when there is no gate voltage applied. If we refer to the Fig.1b, we can see that when the device is in equilibrium without any external voltage applied, there exists the 2DEG between AlGaN and GaN. Then, if we apply a nonzero drain-source voltage to an AlGaN/GaN HEMT(Fig.2), then the current will flow between two terminals, which means the device is normally-on. Only by applying negative voltage to deplete the channel, the device will turn-off(Fig.1c). Hence the name depletion-mode.

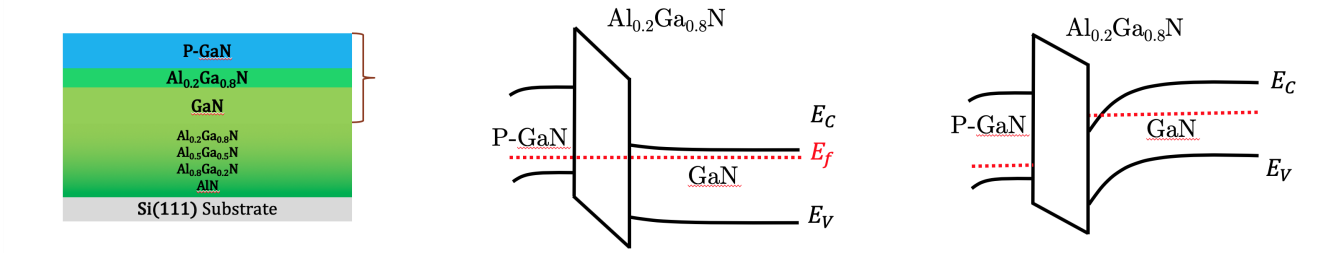
Depletion-mode devices make it significantly hard to design electronic circuits with those devices, as we need to take care of turning off the devices with negative voltage in addition to their normal operation with zero and positive voltages.

2.4 P-GaN/AlGAN/GaN HEMT and Enhancement-mode Devices

Many people have tried to solve this depletion-mode nature of AlGaN/GaN HEMTs and make the devices **normally-off** or **enhancement-mode(e-mode)**. Enhancement-mode devices are the devices that would not flow electric current when no positive gate voltage is applied. People like Huang et al.[3] and Lanford et al.[4] tried recessed gate structures to suppress 2DEG for zero bias. Other techniques such as fluorine plasma treatment by Cai et al.[5] and ferroelectric materials by Lee at al.[6] were also tried.

Another way to achieve an enhancement-mode device would be using materials with proper workfunction to perform **band engineering** and suppress the zero-bias 2DEG. **P-type GaN** doped with Mg acceptors on top of AlGaN/GaN layers can function as such a material[7, 8].

Fig.3a shows the PGaN/AlGaN/GaN heterostructure. This p-type doping can be done using Mg dopants during



(a) PGaN/ AlGaN/ GaN structure with graded $Al_xGa_{1-x}N$ buffer

(b) Band diagram of PGaN/ AlGaN/ GaN heterostructure with zero bias

(c) Band diagram of PGaN/ AlGaN/ GaN heterostructure with positive bias

Figure 3: PGaN/AlGaN/GaN heterostructure

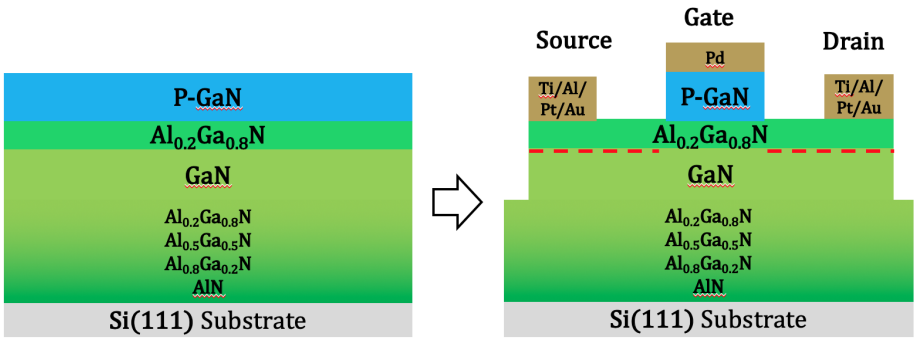


Figure 4: P-GAN/AlGaN/GaN HEMT with Suppressed 2DEG for Zero Bias

the growth of the layer. As can be seen from the band diagram(Fig.3a), the p-type GaN pulls up the Fermi level and depletes the 2DEG even when there is no gate voltage applied. However, since we have not destroyed the environment in which 2DEG of AlGaN/GaN structure can form, we can retrieve the 2DEG by applying positive voltage as in Fig.3c. If we use this heterostructure to build a transistor (Fig.4), we can have an enhancement-mode transistor utilizing the high-performance 2DEG channel of AlGaN/GaN heterostructure.

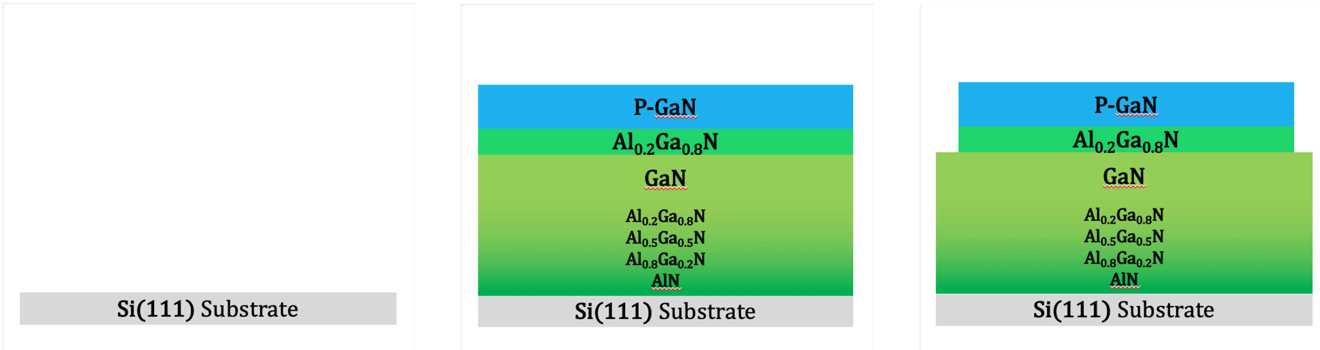
For us, the primary advantages of using a P-GaN layer are two-fold; first of all, it can be done in the MOCVD machine itself without needs for additional tools. Secondly, current industry standards are using the P-GaN for their own enhancement-mode devices, thus we can keep up with the trend. Currently, SNF has recipes for successful growth of AlGaN/GaN heterojunction layers in the MOCVD process. However, we have lacked the ability to add dopants (in particular, p-type) to this process to grow a layer of P-GaN. Therefore, our MOCVD-based GaN HEMTs that SNF could make were depletion-mode devices. However, now we have a P-GaN recipe for LEDs in SNF. We hope to transfer this P-GaN recipe to the depletion-mode device we have and combine them together to make an enhancement-mode transistor.

2.5 Objective

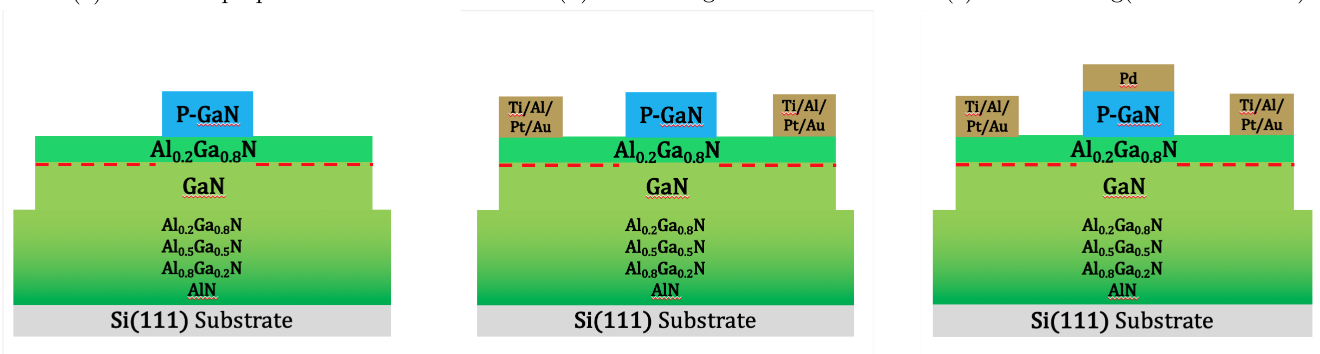
The primary objective of the project will be the development of a recipe of P-GaN/AlGaN/GaN e-mode HEMTs (using Mg as dopant) in MOCVD, as seen in the Fig. 4. In order to do so, we need to characterize our P-GaN using Hall measurements and cross sectional SEM to verify the electrical properties and growth rate. Therefore, we will be able to optimize the the thickness (and possibly the doping level) of P-GaN layer for better performance of the transistors. The expected trade-off is that, the thicker the P-GaN layer, the better suppression of the zero-bias but the lower gate control we have.

This project also hopes to expand the testing of the devices formed above to see durability and reliability at higher temperatures (up to 700 °C) with the SPI system probe analyser in XLab. The main interest of the XLab in the GaN devices resides in the harsh environment(high-temperature, high-radiation) applications such as space missions[9]. However, there is little literature available on how P-GaN device performance changes for higher temperatures.

3 Device Fabrication Method



(a) Substrate preparation (b) MOCVD growth (c) Mesa etching(device isolation)



(d) P-GaN etching(gate definition) (e) Ohmic contact formation(S,D) (f) Schottky contact formation(G)

Figure 5: Device fabrication steps summary

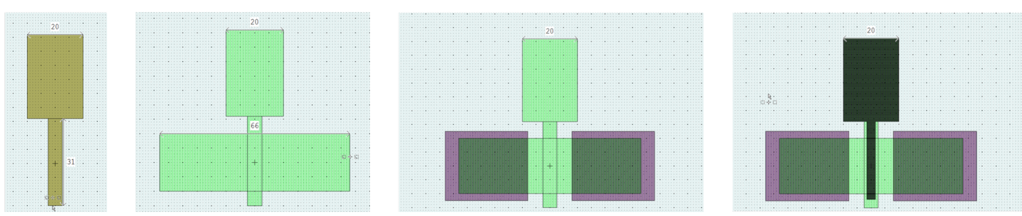
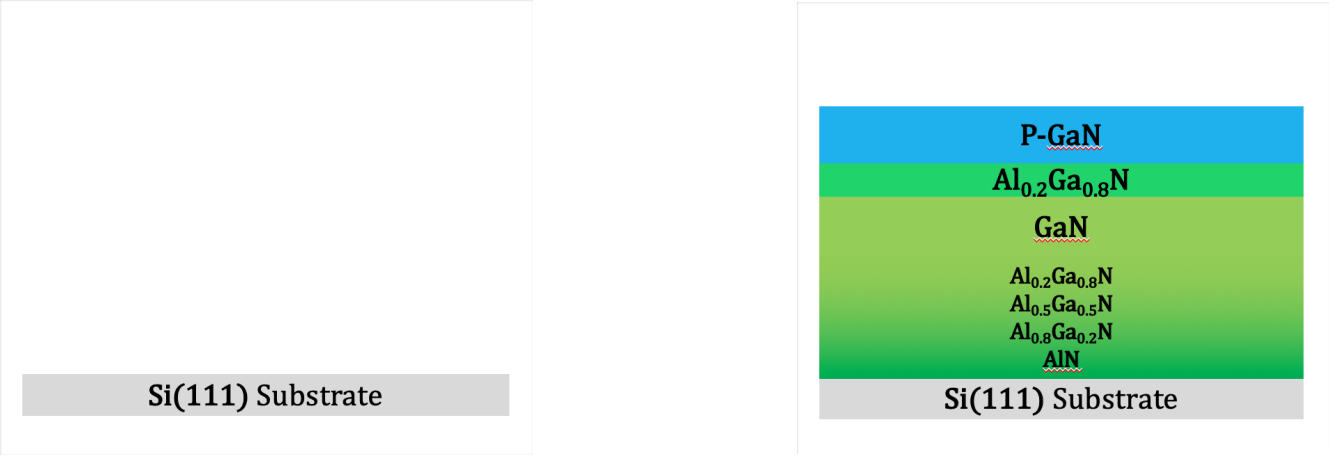


Figure 6: Example mask designs for p-GaN etch, mesa(active region) etch, ohmic contact, and schottky contact from the left to the right. The detailed dimensions and overlaps were actually varied for experiments.

Fig.5 gives us a summary of the whole fabrication process. We prepare a **silicon (111) wafer** as the base substrate. Then we grow the layers using **MOCVD**. After that, we use 2 different masks for etching steps. Fist, we do the device isolation etch (also called **mesa etching**). Second, we do the **P-GaN etching** which leaves p-doped GaN only in the gate area. Next steps are to deposit the source, drain and gate metal contacts. The **Ohmic contacts(S,D)** are formed first, then comes the **Schottky contacts(G)**. We will illustrate the details in the following subsections.

3.1 MOCVD Growth Of Layers



(a) Sample before MOCVD growth

(b) Sample after MOCVD growth

Figure 7: MOCVD growth of buffer layers, GaN layer, AlGaN layer and PGaN layer

One of the benefits of this PGaN/AlGaN/GaN heterosturcture is that the whole growth can be done at once. However, unlike silicon, we cannot rely on conventional growth processes such as Czochralski pull method, as GaN would decompose into Ga and N if heated.

The way GaN and other complex III-V systems are grown is using a method called **metal organic chemical vapor deposition (MOCVD)**. This method is also known as organometallic vapor-phase epitaxy (OMVPE) or Metalorganic vapor-phase epitaxy (MOVPE). Inside its chamber, the reactant gases which are organometallic(oranic + metal) chemicals, are combined at high temperatures through chemical interaction, resulting in the deposition of materials, mainly III-V compounds. For example, the deposition of a GaM layer can be carried out by the following reaction.

$$\mathrm{Ga(CH_3)_3 + NH_3 \rightarrow 3CH_4 + GaN} \tag{4}$$

Since GaN wafers are not readily available, primary growth of GaN is on Si (111) or SiC and sapphire. The lattice mismatch between Si (111) and GaN is around 17%. To accommodate this lattice mismatch and growth of relatively uniform crystals, a graded buffer layer is grown . This buffer layer consists of $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N}$ where x varies from 0 to 0.2, 0.5, 0.8, as can be seen in Fig.7.On top of these layers, regular AlGaN/GaN layers are grown to form the 2DEG. (The 2DEG AlGaN is $\mathrm{Al}_{0.2}\mathrm{Ga}_{0.8}\mathrm{N}$.) This is basically a regular d-mode HEMT without contacts.

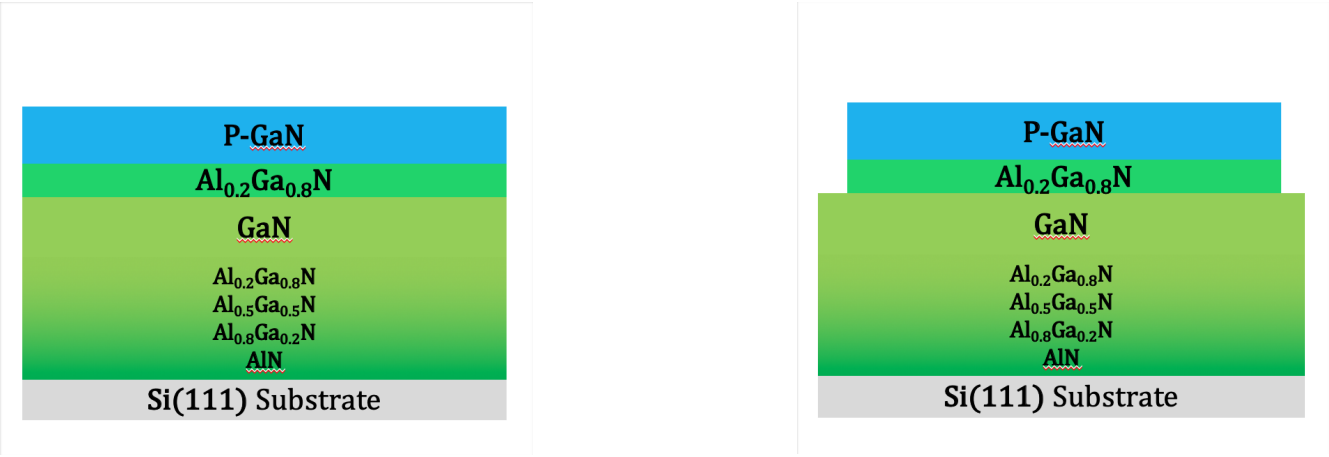
On top of these layers, we grow an Mg-doped GaN layer(P-GaN). One of the benefits of MOCVD is that we can introduce dopants during the growth of the material, which means we can avoid using ion-implantation that can damage the layer. This cap layer is supposed to be only under the gate, hence the rest of this layer is etched out later. Literature states values for P-GaN thickness od 50-80 nm for e-mode devices.

Although MOCVD growth is an incredibly complex procedure and creating new recipes require extensive knowledge of the MOCVD processes, we here list the important aspects of the recipe used by us to grow GaN and PGaN. These recipes built upon existing recipes at SNF and with the help of our mentor, Dr. Xu, we combined them and altered them based on the thicknesses desired and measured subsequently. Of these, the most important is arguably the time for each growth. We estimate it to be a linear function between thickness of the layer and time the layer is deposited (i.e. longer the time for that layer the thicker the layer). All units are in Si (nm, seconds and °C).

General
TMGa 5°C, 1900mbar (CS16264 was 5°C, 1300 mbar)
TMAl 20°C, 1300mbar
SiH4, 100ppm in H2
Cp2Mg: 15C
Baking
variable Bake_Temp = 987;
variable Bake_ZnA = 53.8+5;
variable Bake_ZnB = 62.6;
variable Bake_ZnC = 65.4;
variable Bake_Time = 300;
variable Bake_Time_SiH4 = 600;
variable Bake_Press = 300;
variable Bake_SiH4_Flow = 80;
GaN
variable GaN_Press = 200;
variable GaN_TMGa_Flow = 40.5;
variable GaN_NH3_Flow = 6000;
variable GaN_Time = 500;#aim to get 200nm
variable Total_Flow_GaN = 12000;
variable GaN_Temp = 1270;
variable GaN_ZnA = 58+5;
variable GaN_ZnB = 65;
variable GaN_ZnC = 62;
variable GaN_Temp_Final = 1295;
variable GaN_ZnA_Final = 58.5+5;
variable GaN_ZnB_Final = 65.5;
variable GaN_ZnC_Final = 62;
AlGaN
parameter runtime TwoDEG_Temp = 1280;
parameter runtime TwoDEG_Time = 400*0.9*2/3;#AIM AT 20nm
parameter runtime TwoDEG_Press = 100;
parameter runtime TwoDEG_TMGa_Flow = 7.6;
parameter runtime TwoDEG_TMAl_Flow = 5.5; #25%
parameter runtime TwoDEG_NH3_Flow = 1340/2; #half Gr.
parameter runtime TwoDEG_Cap_Time = 30;
parameter runtime TwoDEG_AlN_Time = 40;
GaN + Mg Doping
variable GaN_Temp_pdoping = 1200; #aim at 1025C surface temp in H2
variable pGaN_Press = 400;#200;
variable pGaN_TMGa_Flow = 5; #40.5/3;
variable pGaN_NH3_Flow = 6000/3;
variable pGaN_Time = 680*4*100/200*50/150*3;#was getting 17∼20nm for sj#1, aim at 50-60nm; was getting 150nm, aim at 50nm; was ∼200nm, aim at 100nm
variable Total_Flow_pGaN = 12000;
variable pGaN_ZnA = 58+5;
variable pGaN_ZnB = 65;
variable pGaN_ZnC = 62;
parameter runtime pGaN_Cp2Mg_source = 200;

Table 3: PGaN/AlGaN/GaN Heterostructure MOCVD Parameters

3.2 Mesa Etching (Device Isolation)



(a) Sample before mesa etching

(b) Sample after mesa etching

Figure 8: Mesa etching to leave AlGaN/GaN heterostructure only for active area

Mesa etching(Fig.8) is a step to isolate the active regions of the devices. The possible current path of the PGaN/AlGaN/GaN structure either highly-doped p-type GaN layer or the 2DEG at the AlGaN/GaN interface. If we etch through PGaN and AlGaN, we remove both of them. This step does not require exact etch depth as long as all PGaN and AlGaN are removed for non-active area, and hence overetching is recommended in general. For example, if P-GaN thickness is 60 nm and AlGaN thickness is 20 nm, then the total etch depth should be 80 nm or above. Overetching by 30 60 nm can guarantee the device isolation without problems. Also, since this is the first etching step, this step inscribes the alignment markers for future etchings and metal deposition. This step comprises of two substeps: mesa lithography and mesa etching. **Mesa lithography**(Table.5) is the substep to transfer a pattern on our sample, **mesa etching**(Table.6) is the substep in which the sample goes through actual dry etching.

The table.4 shows the recipes of etching we used. The whole etching step consists of (1) pumping (2) 5-second striking (3) main etching (4) pumping. The purpose of adding a strike step is to insert BCl_3 gas into the chamber to remove the oxide on top.

Recipe Name	**Strike**	**Main Etch G**	**Main Etch Y**
Forward Power	150 W	50 W	30 W
ICP Power	250 W	250 W	250 W
Strike Pressure	20 mTorr	20 mTorr	20 mTorr
APC Set Pressure	10 mTorr	5 mTorr	10 mTorr
He Pressure	7mTorr	7mTorr	7mTorr
Gas	BCl_3 20 sccm Ar 20 sccm	Cl_2 30 sccm Ar 10 sccm O_2 2 sccm	BCl_3 25 sccm Cl_2 10 sccm
PGaN rate	-	-	19 nm/min
AlGaN rate	-	-	-
GaN rate	74 nm/min	60 nm/min	20 nm/min

Table 4: Etching Recipe

Unfortunately, many of the etch rate characterization turned out to be analyzed with experimental mistakes and they are being re-characterized.

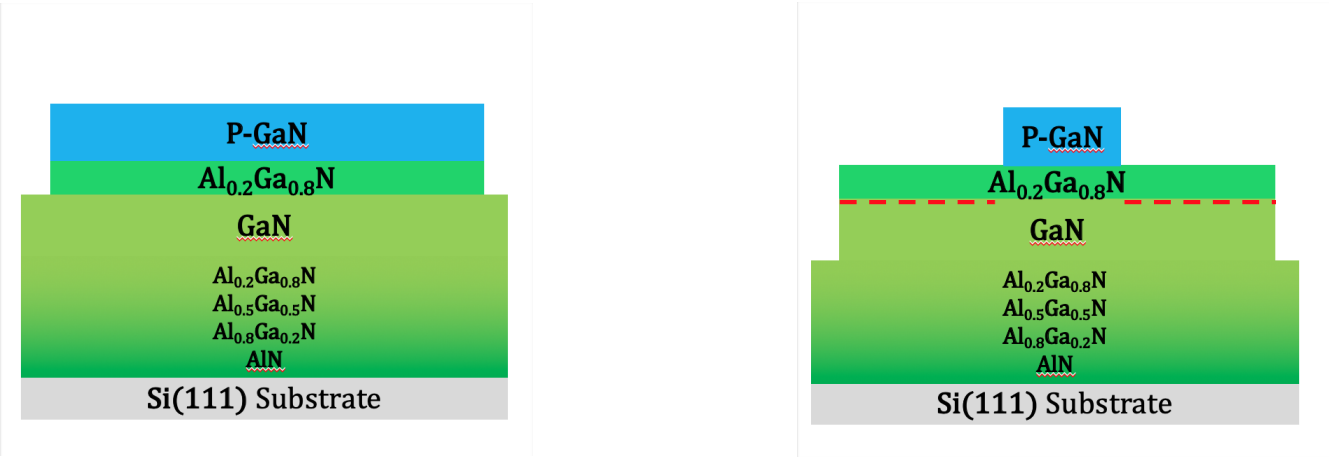
Process Step	Equipment	Temp.	Time	Recipe
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
Blow-drying	wbflexsolv	RT	10 sec	Blow-dry the sample.
HCl Cleaning	wbflexcorr	N/A	20 sec	Clean the sample using diluted HCl (5:1). Dip the sample in the solution which is hot from dilution.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
HDMS	yes	N/A	35 min	Run the pre-set recipe for HDMS coating of the sample.
Photoresist Spinning	headway2	RT	60 sec	Using a 1 um filter and a syringe, drop SPR3612 on top of the sample. Spin it using headway in 5000 rpm for 60 seconds.
Pre-bake	hot plate	90C	1 min	Place the sample on the hot plate.
Exposure	heidelberg	RT	N/A	Expose the sample using the mask for mesa etching. Make sure the mask is inverted, so that the drawn part is protected.
Post-bake	hot plate	115C	1 min	Place the sample on the hot plate.
Development	headway2 bench	RT	30 sec	Prepare two beakers, one filled with DI water and the other filled with MF26A developer. Using a teflon basket, dip the sample in MF26A for 30 seconds, then rinse it using DI water.
Blow-drying	headway2 bench	RT	10 sec	Blow-dry the sample.
Development Check	optical microscope	RT	N/A	Using one of the optical microscopes, check if the photoresist is developed correctly. If not, develop it for additional time. If it still fails, then go back to acetone cleaning.
Hard-bake	hot plate	115C	5 min	Place the sample on the hot plate.

Table 5: Mesa Lithography

Process Step	Equipment	Temp.	Time	Recipe
Etcher Cleaning	ox-35	N/A	15 min	Run recipe "OPT 3-step Clean" to clean inside the etcher chamber. Use a dummy wafer.
Etcher Conditioning	ox-35	N/A	15 min	Run the GaN etching recipe(e.g. "XLab PGaN Y") to condition inside the etcher chamber. Use a dummy wafer.
Etching	ox-35	N/A	Calc.	Dry etch the sample. The duration of etching should be calculated by desired etch depth(t_{PGaN},t_{AlGaN}) divided by the recipe etch rate(r_{PGaN},r_{AlGaN}). The minimum etching time τ_{etch} can be calculated as the sum of $\tau_{PGaN} = t_{PGaN}/r_{PGaN}$ and $\tau_{AlGaN} = t_{AlGaN}/r_{AlGaN}$ (e.g. Assume the PGaN thickness and the AlGaN thickness are 60 nm and 20 nm respectively. Then with "XLab PGaN Y"'s etch rates, namely, PGaN 20 nm/min and AlGaN 20 nm/min, the total etching time is 60/20+20/20 = 4 [min]. We can overetch to about 5 min.)
SRS-100 Cleaning	wbflexcorr	60C	20 min	Clean the sample using SRS-100(N-Methyl-2 Pyrrolidone 60%, Tetramethylen Sulfone 30%, Isopropanolamine 10%). Dip the sample in the solution using a teflon basket. After 20 minutes, dip the sample in DI water for 1 minute and rinse the sample again with flowing DI water.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.

Table 6: Mesa Etching

3.3 P-GaN Etching (Gate Definition)

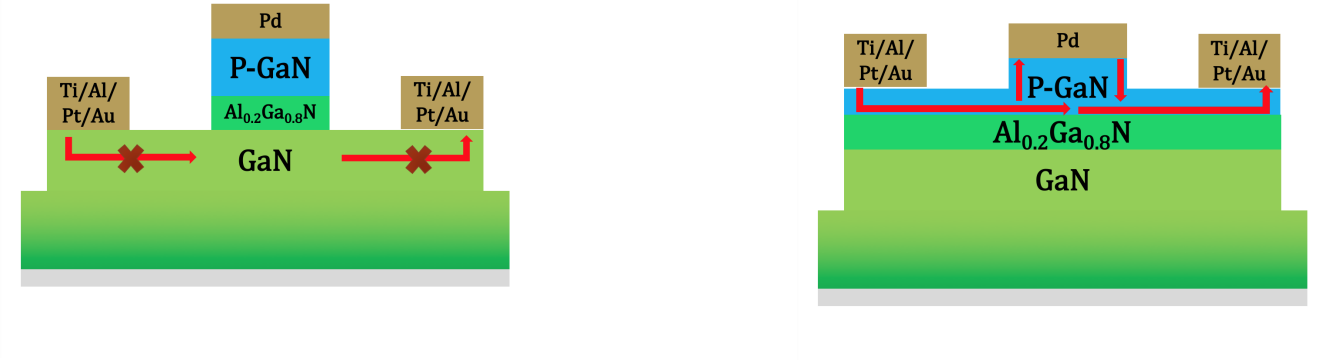


(a) Sample before PGaN etching

(b) Sample after PGaN etching

Figure 9: PGaN etching to leave PGaN layer only for the gate area

PGaN etching(Fig.9) is a step to define the gate areas of the devices. This step removes all the PGaN left after mesa etching, except for the gate area where 2DEG should be normally-suppressed. This step does require *exactly controlled etching*, and overetching of only about 0 5 nm is recommended. For example, if P-GaN thickness is 60 nm, then the total etch depth should be 60-65 nm. Here we illustrate how wrong etching can fail our devices.



(a) AlGaN layer removed after too much overetching

(b) PGaN layer shorts metal contacts excessive underetching

Figure 10: PGaN etching failure due to erroneous etch depth control.

Fig.10a shows a device where the overetching removed AlGaN layer. In this case, since the 2DEG of AlGaN/GaN heterostructure is lost and instrinsic GaN is insulating, we have no current path between source and drain. Fig.10b shows when the PGaN is underetched. Since the metal contacts are shorted by the highly-doped p-type GaN layer, the device does not function as a transistor and we see very high gate leakage. (Note that, though the gate is a Schottky contact instead of an Ohmic contact, it does not completely block current flow for positive bias.) Hence we need extremely well-controlled etching.

This step comprises of 5 substeps: PGaN test lithography, PGaN test etching, PGaN test, PGaN lithography and PGaN etching. **PGaN test lithography**(Table.5) is the substep to transfer a test pattern on a dummy

sample, and **PGaN test etching**(Table.6) performs the dry etching. Then during **PGaN test**(Table.6), we use SEM and/or AFM to confirm the etching. Those three steps are to confirm the etch rate, as the etch rate is a time-variant function of the tool condition and the tool history, etc. If the etch rate was recently verified then these three step might be omitted. The main substeps are pretty much the same as the mesa etching: **PGaN lithography**(Table.6) and **PGaN etching**(Table.6)

Process Step	Equipment	Temp.	Time	Recipe
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
Blow-drying	wbflexsolv	RT	10 sec	Blow-dry the sample.
HCl Cleaning	wbflexcorr	N/A	20 sec	Clean the sample using diluted HCl (5:1). Dip the sample in the solution which is hot from dilution.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
HDMS	yes	N/A	35 min	Run the pre-set recipe for HDMS coating of the sample.
Photoresist Spinning	headway2	RT	60 sec	Using a 1 um filter and a syringe, drop SPR3612 on top of the sample. Spin it using headway in 5000 rpm for 60 seconds.
Pre-bake	hot plate	90C	1 min	Place the sample on the hot plate.
Exposure	heidelberg	RT	N/A	Expose the sample using the etch rate test.
Post-bake	hot plate	115C	1 min	Place the sample on the hot plate.
Development	headway2 bench	RT	30 sec	Prepare two beakers, one filled with DI water and the other filled with MF26A developer. Using a teflon basket, dip the sample in MF26A for 30 seconds, then rinse it using DI water.
Blow-drying	headway2 bench	RT	10 sec	Blow-dry the sample.
Development Check	optical microscope	RT	N/A	Using one of the optical microscopes, check if the photoresist is developed correctly. If not, develop it for additional time. If it still fails, then go back to acetone cleaning.
Hard-bake	hot plate	115C	5 min	Place the sample on the hot plate.

Table 7: PGaN test lithography

Process Step	Equipment	Temp.	Time	Recipe
Etcher Cleaning	ox-35	N/A	15 min	Run recipe "OPT 3-step Clean" to clean inside the etcher chamber. Use a dummy wafer.
Etcher Conditioning	ox-35	N/A	15 min	Run the GaN etching recipe(e.g. "XLab PGaN Y") to condition inside the etcher chamber. Use a dummy wafer.
Etching	ox-35	N/A	Calc.	Dry etch the sample. The duration of etching should be calculated by desired etch depth(t_{PGaN}) divided by the recipe etch rate(r_{PGaN}). The etching time τ_{etch} can be calculated as $\tau_{PGaN} = t_{PGaN}/r_{PGaN}$ (e.g. Assume the PGaN thickness is 60 nm. Then with "XLab PGaN Y"'s etch rate 20 nm/min and 3 nm overetching, the total etching time is 63/20 = 3 [min] 9 [sec].)
SRS-100 Cleaning	wbflexcorr	60C	20 min	Clean the sample using SRS-100(N-Methyl-2 Pyrrolidone 60%, Tetramethylen Sulfone 30%, Isopropanolamine 10%). Dip the sample in the solution using a teflon basket. After 20 minutes, dip the sample in DI water for 1 minute and rinse the sample again with flowing DI water.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.

Table 8: PGaN test etching

Process Step	Equipment	Temp.	Time	Recipe
AFM Test	XE-70	RT	N/A	Check if the test sample pattern has the right etch depth we calculated.
FIB Test	db235	RT	N/A	Check if the test sample pattern has the right etch depth we calculated.

Table 9: PGaN test

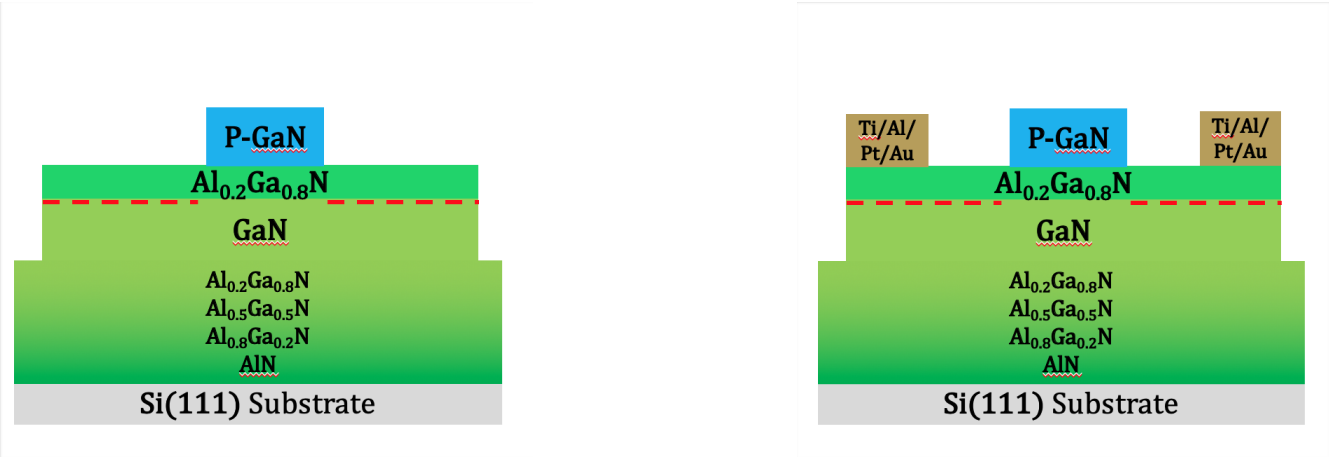
Process Step	Equipment	Temp.	Time	Recipe
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
Blow-drying	wbflexsolv	RT	10 sec	Blow-dry the sample.
HCl Cleaning	wbflexcorr	N/A	20 sec	Clean the sample using diluted HCl (5:1). Dip the sample in the solution which is hot from dilution.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
HDMS	yes	N/A	35 min	Run the pre-set recipe for HDMS coating of the sample.
Photoresist Spinning	headway2	RT	60 sec	Using a 1 um filter and a syringe, drop SPR3612 on top of the sample. Spin it using headway in 5000 rpm for 60 seconds.
Pre-bake	hot plate	90C	1 min	Place the sample on the hot plate.
Exposure	heidelberg	RT	N/A	Expose the sample using the mask for PGaN etching. Make sure the mask is inverted, so that the drawn part is protected.
Post-bake	hot plate	115C	1 min	Place the sample on the hot plate.
Development	headway2 bench	RT	30 sec	Prepare two beakers, one filled with DI water and the other filled with MF26A developer. Using a teflon basket, dip the sample in MF26A for 30 seconds, then rinse it using DI water.
Blow-drying	headway2 bench	RT	10 sec	Blow-dry the sample.
Development Check	optical microscope	RT	N/A	Using one of the optical microscopes, check if the photoresist is developed correctly. If not, develop it for additional time. If it still fails, then go back to acetone cleaning.
Hard-bake	hot plate	115C	5 min	Place the sample on the hot plate.

Table 10: PGaN lithography

Process Step	Equipment	Temp.	Time	Recipe
Etcher Cleaning	ox-35	N/A	15 min	Run recipe "OPT 3-step Clean" to clean inside the etcher chamber. Use a dummy wafer.
Etcher Conditioning	ox-35	N/A	15 min	Run the GaN etching recipe(e.g. "XLab PGaN Y") to condition inside the etcher chamber. Use a dummy wafer.
Etching	ox-35	N/A	Calc.	Dry etch the sample. The duration of etching should be calculated by desired etch depth(t_{PGaN}) divided by the recipe etch rate(r_{PGaN}). The etching time τ_{etch} can be calculated as $\tau_{PGaN} = t_{PGaN}/r_{PGaN}$ (e.g. Assume the PGaN thickness is 60 nm. Then with "XLab PGaN Y"'s etch rate 20 nm/min and 3 nm overetching, the total etching time is 63/20 = 3 [min] 9 [sec].)
SRS-100 Cleaning	wbflexcorr	60C	20 min	Clean the sample using SRS-100(N-Methyl-2 Pyrrolidone 60%, Tetramethylen Sulfone 30%, Isopropanolamine 10%). Dip the sample in the solution using a teflon basket. After 20 minutes, dip the sample in DI water for 1 minute and rinse the sample again with flowing DI water.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.

Table 11: PGaN etch

3.4 Ohmic Contact(S,D) Formation



(a) Sample before Ohmic contact formation

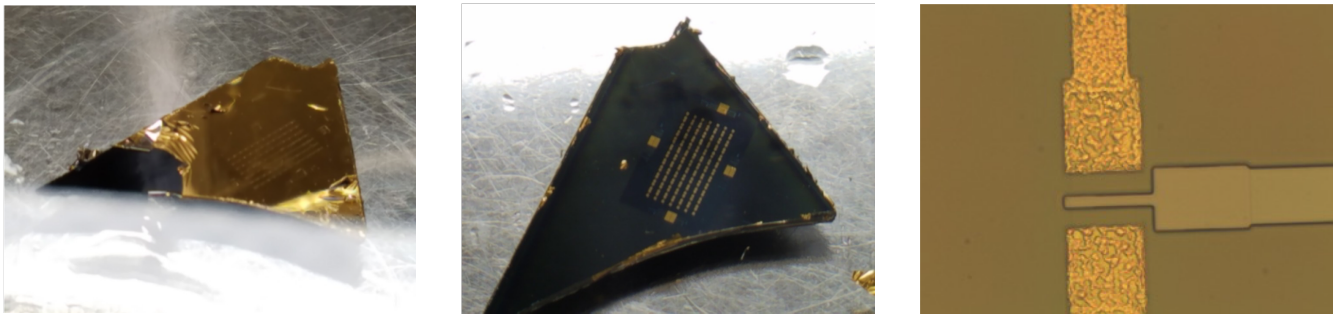
(b) Sample after Ohmic contact formation

Figure 11: Ohmic contacts formed for the source and drain contacts

Now we need to form source and drain contacts(Fig.11). This should be done before the gate contact which is a Schottky contact, as the ohmic contact formation requires a rapid thermal annealing(RTA). The mechanism in which we form an Ohmic contact that connects the metal and the 2DEG underneath the AlGaN layer can be summaraized as following.

First, we deposit Ti(20 nm)/Al(100 nm)/Pt(80 nm)/Au(40 nm). This is done by the famous lift-off process, in which we coat the sample with photoresist-liftoff dual layer and remove the part for metal deposition. Then we evaporate the metal, then remove the dual layer hence the unwanted metal is removed with the layer. This removal is done by dipping the sample in dedicated solvents(Fig.12a,12b). Then when we heat it at a temperature as high as 850 °C, the formation of TiN and n-type GaN made through the diffusion of Al and N results in an Ohmic contact[10]. You can see the RTA-treated metals in Fig.12c

Therefore, this step consists of 3 substeps, the lithography, the metal evaporation, and the RTA. For metals, in addition to the usual photoresist SPR3612, we use another layer of LOL 2000. This dual layer of lift-off layer/photoresist layer gives a slight undercut during development, and help the metal deposition.



(a) Lift-off process. 24 hours in solvent

(b) Lift-off process completed.

(c) Rapid thermal annealing(RTA)

Figure 12: Lift-off and RTA of Ohmic contacts

Process Step	Equipment	Temp.	Time	Recipe
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
Blow-drying	wbflexsolv	RT	10 sec	Blow-dry the sample.
HCl Cleaning	wbflexcorr	N/A	20 sec	Clean the sample using diluted HCl (5:1). Dip the sample in the solution which is hot from dilution.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
HDMS	yes	N/A	35 min	Run the pre-set recipe for HDMS coating of the sample.
Lift-off Layer Spinning	headway2	RT	30 sec	Using a 1 um filter and a syringe, drop LOL2000 on top of the sample. Spin it using headway in 3000 rpm for 30 seconds.
Lift-off-bake	hot plate	170C	5 min	Place the sample on the hot plate.
Photoresist Spinning	headway2	RT	60 sec	Using a 1 um filter and a syringe, drop SPR3612 on top of the sample. Spin it using headway in 5000 rpm for 60 seconds.
Pre-bake	hot plate	90C	1 min	Place the sample on the hot plate.
Exposure	heidelberg	RT	N/A	Expose the sample using the mask for Ohmic contact. This time the mask is *non-inverted*, so that the drawn part is removed and metal can fill in this vacancy.
Post-bake	hot plate	115C	1 min	Place the sample on the hot plate.
Development	headway2 bench	RT	30 sec	Prepare two beakers, one filled with DI water and the other filled with MF26A developer. Using a teflon basket, dip the sample in MF26A for 30 seconds, then rinse it using DI water.
Blow-drying	headway2 bench	RT	10 sec	Blow-dry the sample.
Development Check	optical microscope	RT	N/A	Using one of the optical microscopes, check if the photoresist is developed correctly. If not, develop it for additional time. If it still fails, then go back to acetone cleaning.
Hard-bake	hot plate	115C	5 min	Place the sample on the hot plate.
De-scum	drytek2	N/A	2 min	Run drytek2 descum recipe for 2 minutes to remove any organics left.

Table 12: Ohmic lithography

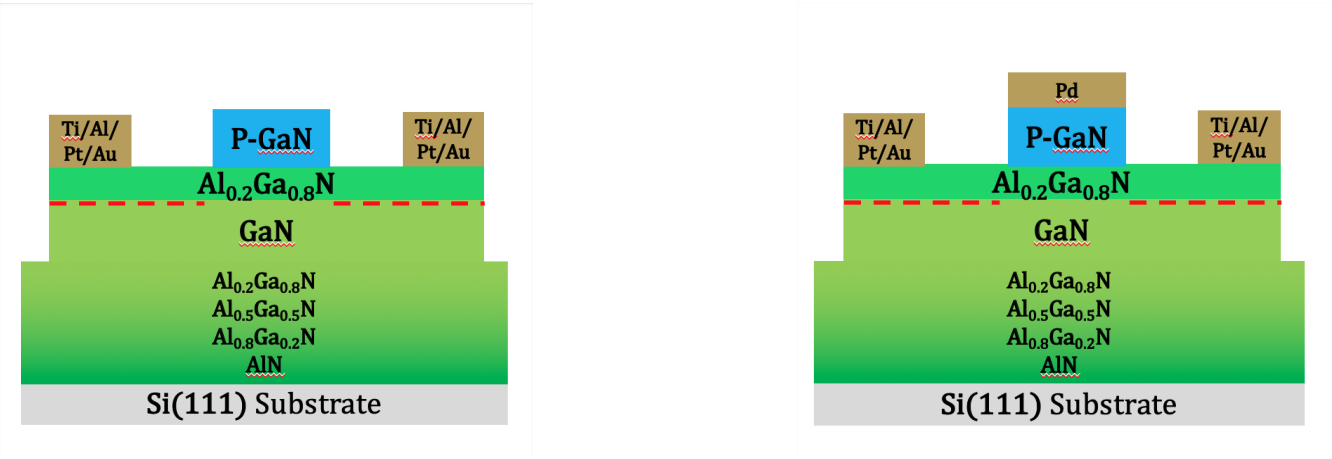
Process Step	Equipment	Temp.	Time	Recipe
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
Evaporation	aja-evap	N/A	N/A	Deposit metals:Ti(20 nm)/Al(100 nm)/Pt(80 nm)/Au(40 nm). Make sure you wait for 10 minutes between each metal deposition.
Lift-off	wbflexsolv	RT	24 hr	Put the sample in a beaker filled with Remover 1165 solvent. Since the metal layer is thick, dipping the sample in the solvent alone might not remove the lift-off layer easily. Peeling off the layer after 24 hours can help.
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
SRS-100 Cleaning	wbflexcorr	60C	20 min	Clean the sample using SRS-100(N-Methyl-2 Pyrrolidone 60%, Tetramethylen Sulfone 30%, Isopropanolamine 10%). Dip the sample in the solution using a teflon basket. After 20 minutes, dip the sample in DI water for 1 minute and rinse the sample again with flowing DI water.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.

Table 13: Ohmic evaporation

Process Step	Equipment	Temp.	Time	Recipe
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
RTA	aw610	850C	30 sec	Recipe:P_850N2 Gas: N_2 10 sccm Ramping: 0C to 850C (20 sec) Steady: 850C (30 sec) Cooling 0C (60 sec)

Table 14: Ohmic rapid thermal annealing

3.5 Schottky Contact(G) Formation



(a) Sample before Schottky contact formation

(b) Sample after Schottky contact formation

Figure 13: Schottky contact formed for the gate

The gate metal deposition(Fig.13) is the last step. Here, we form Schottky contact instead of Ohmic contact. Of course, when positive gate voltage is applied, the Schottky contact cannot block much current. However, it still gives much less gate leakage compared to Ohmic contacts. In general, high-workfunction metals such as Pt or Pd will do. Here we used the Pd. The procedure is pretty much the same as Ohmic contact, however, this time we only deposit 50 nm of Pd metal and do not perform any RTA.

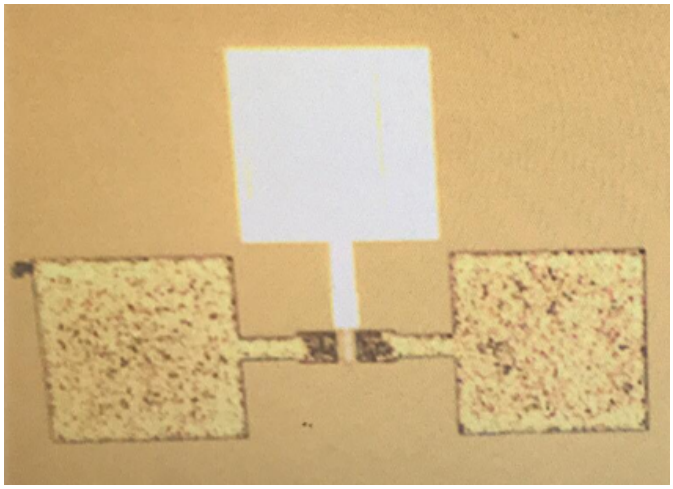


Figure 14: Schottky contact formed(white metal)

Process Step	Equipment	Temp.	Time	Recipe
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
Blow-drying	wbflexsolv	RT	10 sec	Blow-dry the sample.
HCl Cleaning	wbflexcorr	N/A	20 sec	Clean the sample using diluted HCl (5:1). Dip the sample in the solution which is hot from dilution.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
HDMS	yes	N/A	35 min	Run the pre-set recipe for HDMS coating of the sample.
Lift-off Layer Spinning	headway2	RT	30 sec	Using a 1 um filter and a syringe, drop LOL2000 on top of the sample. Spin it using headway in 3000 rpm for 30 seconds.
Lift-off-bake	hot plate	170C	5 min	Place the sample on the hot plate.
Photoresist Spinning	headway2	RT	60 sec	Using a 1 um filter and a syringe, drop SPR3612 on top of the sample. Spin it using headway in 5000 rpm for 60 seconds.
Pre-bake	hot plate	90C	1 min	Place the sample on the hot plate.
Exposure	heidelberg	RT	N/A	Expose the sample using the mask for Schottky contact. This time the mask is *non-inverted*, so that the drawn part is removed and metal can fill in this vacancy.
Post-bake	hot plate	115C	1 min	Place the sample on the hot plate.
Development	headway2 bench	RT	30 sec	Prepare two beakers, one filled with DI water and the other filled with MF26A developer. Using a teflon basket, dip the sample in MF26A for 30 seconds, then rinse it using DI water.
Blow-drying	headway2 bench	RT	10 sec	Blow-dry the sample.
Development Check	optical microscope	RT	N/A	Using one of the optical microscopes, check if the photoresist is developed correctly. If not, develop it for additional time. If it still fails, then go back to acetone cleaning.
Hard-bake	hot plate	115C	5 min	Place the sample on the hot plate.
De-scum	drytek2	N/A	2 min	Run drytek2 descum recipe for 2 minutes to remove any organics left.

Table 15: Schottky lithography

Process Step	Equipment	Temp.	Time	Recipe
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
Evaporation	aja-evap	N/A	N/A	Deposit metals:Pd(50 nm).
Lift-off	wbflexsolv	RT	24 hr	Put the sample in a beaker filled with Remover 1165 solvent. Since the metal layer is thick, dipping the sample in the solvent alone might not remove the lift-off layer easily. Peeling off the layer after 24 hours can help.
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
SRS-100 Cleaning	wbflexcorr	60C	20 min	Clean the sample using SRS-100(N-Methyl-2 Pyrrolidone 60%, Tetramethylen Sulfone 30%, Isopropanolamine 10%). Dip the sample in the solution using a teflon basket. After 20 minutes, dip the sample in DI water for 1 minute and rinse the sample again with flowing DI water.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.

Table 16: Schottky evaporation

4 Analysis

4.1 PGaN Layer Growth Analysis

MOCVD growth of layers(Fig.7) is a significantly important step, as if we do not grow AlGaN and PGaN layers properly, we might completely lose 2DEG instead of suppressing it. Growth of $Al_xGa_{1-x}N$ and GaN has been done at Stanford for years. Therefore we have confidence in having reasonable control over those layers' thicknesses. However, Mg-doped GaN is relatively new, with different temperature, pressure etc. Therefore, understanding the PGaN growth including the growth rate as well as the doping level was very important.

To confirm the thicknesses of the grown layer in the MOCVD, we used the SEM. Using Dr Xu's help, we cleaved a small piece with the whole PGaN/ AlGaN/GaN layers grown. The cleaved piece was then put vertically in the SEM (FEI Serion) and we performed a cross-sectional SEM. The fig.15 shows the SEM images of PGaN for different growths.

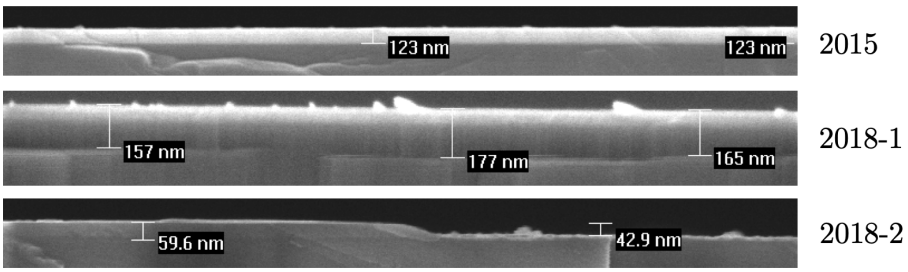


Figure 15: PGaN thickness measured at different times.

With PGaN having much higher conductivity, the SEM images are supposed to clearly show the boundary between PGaN the rest of the layers with good contrast in the colors. AlGaN layer cannot be seen as it is only about 20 nm thick.

For 2015 sample, we estimated the PGaN thickness to be approximately 123 nm. There was a clear boundary between the bright and dark regions, so we assumed that was the P-GaN/AlGaN interface. With this image, we could say that P-GaN growth rate was about 123 nm / (75.7 min) = 1.59 nm / min.

The problem was found from the samples grown in 2018. for about 12.6 minute of growth, we could we some sort of boundaries both at about 157 177 nm below the surface as well as 55 60 nm below the surface. If we think of the latter as the correct boundary between the PGaN and AlGaN, then it is consistent(1.45 1.59 nm/min) with the 2015 analysis while the former give about 3 times higher growth rate of 4.2 4.67 nm/min.Therefore we decided the latter was the correct one and grew later PGaN layers based on this analysis.

4.2 PGaN Layer Electrical Property Analysis

From the P-GaN/AlGaN/GaN structure, we performed the hall measurement to verify whether the 2DEG is suppressed by the P-GaN layer. Using the full model for the hall effect when both the electrons and the holes matter, the Hall coefficient can be written as

$$R_H = \frac{1}{e}\frac{-n\mu_n^2 + p\mu_p^2}{(n\mu_n + p\mu_p)^2} \tag{5}$$

and we know that the total conductivity can be calculated as

$$\sigma_{tot} = \sigma_n + \sigma_p = en\mu_n + ep\mu_p \tag{6}$$

These are 2 equations with 4 variables, the electron mobility μ_n, the electron density n, the hole mobility μ_p and the hole density p. Usually, we ignore one of the carriers and get the mobility and the density of the other carrier. But instead, we can assume the mobility values to be typical values and calculate the densities of both carriers. With the assumption of $\mu_n = 1200\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ and $\mu_p = 10\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, we could find that

$$n_{2DEG} \approx 1 \times 10^{10}\,\mathrm{cm}^{-2}$$
$$p_{PGaN} \approx 1 \times 10^{18}\,\mathrm{cm}^{-3}$$

Without additional treatment such as P-GaN cap layer, the typical value of the 2DEG electron sheet density is about $1 \times 10^{13}\,\mathrm{cm}^{-2}$. We saw an approximately 1,000 times decrease in 2DEG density for zero bias. Therefore, we could conclude that a thick enough P-GaN cap can actually suppress the 2DEG to make the device e-mode.

4.3 Etching Recipe Analysis

Full characterization of etching is also very important, as already described in the fabrication method section. We have two main recipes, one from the literature[8] that is expected to be slow and selective to PGaN than AlGaN. The selectivity and control are required as for fabrication we need to etch through the PGaN layer but stop just before or at the 20 nm thin AlGaN layer. This poses significant issues as etching processes are dependent on a variety of factors: one of them being the cleaning and 'history' of the tool.

We used the Oxford III-V dry plasma etcher with the following two recipes, namely, Y and G. Recipe G is based on what Greco et al. wrote in their paper[8], and recipe Y is based on a former Stanford student Yesheng Yee. Those recipes were already mentioned, but repeated here for convenience.

Recipe Name	**Strike**	**Main Etch G**	**Main Etch Y**
Forward Power	150 W	50 W	30 W
ICP Power	250 W	250 W	250 W
Strike Pressure	20 mTorr	20 mTorr	20 mTorr
APC Set Pressure	10 mTorr	5 mTorr	10 mTorr
He Pressure	7mTorr	7mTorr	7mTorr
Gas	BCl_3 20 sccm Ar 20 sccm	Cl_2 30 sccm Ar 10 sccm O_2 2 sccm	BCl_3 25 sccm Cl_2 10 sccm
PGaN rate	-	-	19 nm/min
AlGaN rate	-	-	-
GaN rate	74 nm/min	60 nm/min	20 nm/min

Table 17: Etching Recipe

The selectivity of G is expected to arrive from the presence of O_2 gas. The oxygen gas should form oxides such as Ga_2O_3 and Al_2O_3 simultaneously when the etching is happening. This slows down further etching. When compared with Ga_2O_3,Al_2O_3 is harder to etch, so we expect selectivity. Too much oxygen gas will lead to no etching. Note, both G and Y have strike steps added in with pure BCl_3 with high power to first attack and break the monolayer of gallium oxide. The strike steps were varied and only short time of it turned out to be necessary. We used 5 seconds of it for maximum linearity.

When we initially had characterized the etching using cross-sectional SEM for G and Y, we estimated the following rates based on the amount etched:

Recipe Name	**Strike**	**Main Etch G**	**Main Etch Y**
PGaN rate	-	14 nm/min	14 nm/min
AlGaN rate	-	7 nm/min	16nm/min
GaN rate	-	14 nm/min	16 nm/min

Table 18: Etching characterization with SEM

However, these rates were never reproduced. We believe the following issues were present in our method for etching. We had done only O_2 cleaning of the chamber, instead of full 3 step (O_2, O_2+SiF_6,Cl_2+BCl_3)version. Moreover, we did conditioning for 5 minutes, which can be short. Since there can be abnormal etching due to the history of the tool, we had to provide enough conditioning. And our measurement was done only once for the sake of time and money. That is, unfortunately, our characterization was innately hard to be reproduced. Lastly, we

used a crossectional SEM for the measurement of etch depths, which could've resulted in incorrect measurement (same cleaving issues and angle issues as above).

Learning from our mistakes, we made a more concrete DOE to better understand the etch rates for Y and G. We made 12 samples of GaN and created a better-checkered mask that allowed us to probe the etch depth. Prior to etching we also performed a three-step clean as mentioned above. This was followed by 15-minute conditioning of the chamber to prime the chamber.

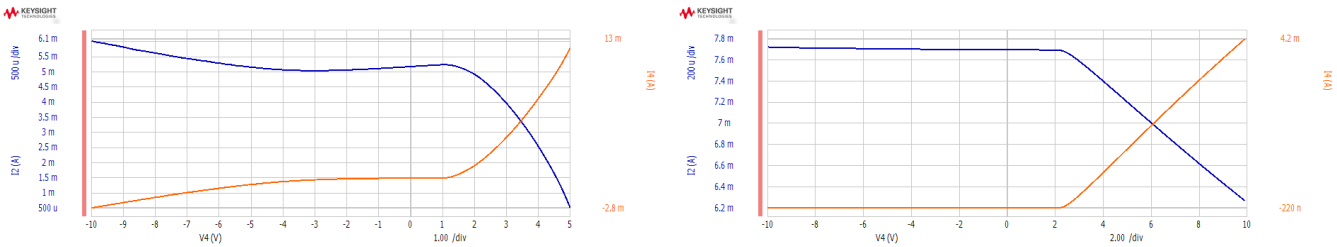
We varied the times from 1, 2 and 5 minutes for Y and G along with the striking step from 0, 10, 30 and 60 seconds. Instead of SEM, we characterised the samples using AFM XE-70 with the help of our classmate, Payton Broaddus and Maryann Tung. AFM provided far more accurate depth profiles than the SEM with more consistency and repeatable measurements. We are going to perform the same characterization on AlGaN and P-GaN to better understand the etch rates for the two materials as well. Table.17 is such a result. This re-characterization is still on-going.

5 Device Measurement

With the fabrication methods and analysis discussed so far, we could manage to finish all the steps for the device fabrication(Fig.16), with PGaN thickness (known to be) 60 nm.

Figure 16: Optical microscope images of the finished devices

However, the IV curves of these devices did not show what we were supposed to see. Fig.17 shows such results. For these measurements, the drain voltage was fixed to 5 V, and the gate voltage was varied between -10 V and 10 V. The source contact was grounded.



(a) $I_D(blue), I_G(red) - V_G$ curve of sample 1

(b) $I_D(blue), I_G(red) - V_G$ curve of sample 2

Figure 17: Drain and gate currents v.s. gate voltage. We can see extremely high gate leakage for positive bias.

This is nothing more than a Schottky diode formed between the gate and the drain. The semiconductor region between D and G were shorted. Then a natural question that arises is whether this channel shorting is in 2DEG or the PGaN. In order to find out, we made a test structure to see how deep we need to etch to completely lose the conductivity between two Ohmic contacts. Since we thought the PGaN thickness was 60 nm and the AlGaN thickness was 20 nm, If we etch by 80 nm the conduction would be completely lost.

However, it was found that until 120 nm etch, the conduction between two Ohmic contacts was not lost. It was found that the PGaN thickness was between 100 nm 160 nm, which is double to triple the target value. This implied not only the etching characterization, but also the growth characterization was erroneously done. Since we only etched 60 nm to remove the PGaN, we could conclude that our devices went through the underetching PGaN failure (Fig.10b)

6 Future Work

6.1 Re-characterization of PGaN Growth and Etching

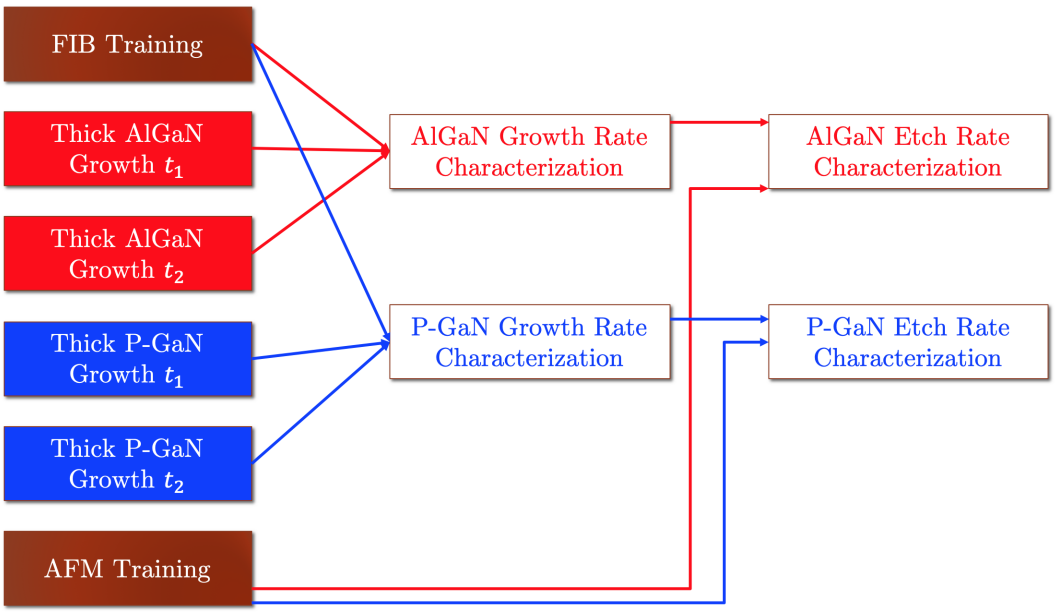


Figure 18: Future plan for re-characterization

Since our failure in the first two sets of devices was due to the un-reproducible etching and growth of PGaN(and maybe AlGaN), we will do the characterization again, after getting trained on AFM and FIB. Fig.18 shows such a plan. We will first grow AlGaN and PGaN samples with thickness 2 3 times larger than our current sample. FIB is supposed to measure the layer thickness (better than regular SEM). After growth characterization is done, we will etch those samples using our etching recipes to re-calculate the rate, These might be supported by SNF as a form of community service project.

7 Financial Report

Our expenditure for fabrication was substantial due to the extensive use of MOCVD to grow layers, and of patterning and dry etching to make them into devices. Also, since both students in this team were new to SNF, the training cost also played a major role in the total expense.

Tool	SJ Fall	AL Fall	Total Fall	SJ Winter	AL Winter	Total Winter	Total Class
aix-ccs	2501.67	320	2821.67	621.66	20	641.66	3463.33
aja-evap	142.87	143.58	286.45	422.25	42.58	464.83	751.28
aw610_r	0	109.16	109.16	48.33	0	48.33	157.49
SNF supply	48	0	48	84	50	134	182
DISCO wafersaw	18.08	205.5	223.58	35.58	0	35.58	259.16
drytek2	0	0	0	172.5	0	172.5	172.5
headway2	0	51.67	51.67	55	145.83	200.83	252.5
heidelberg	0	160	160	565.42	28	593.42	753.42
micromanipulator6000	0	0	0	17.18	25.49	42.67	42.67
Ox-35	80	172.5	252.5	290.01	1555.81	1845.82	2098.32
oxford-rie	160	160	320	0	0	0	320
PT-MTL	0	0	0	160	80	240	240
SNF General	240	160	400	340	160	500	900
wbflexcorr	180	0	180	514.16	0	514.16	694.16
yes	0	0	0	161.67	373.33	535	535
zeiss	0	0	0	533	0	533	533
Total	3370.62	1482.41	4853.03	4020.76	2481.04	6501.8	**11354.83**

8 Conclusion

Thanks to sincere support of SNF and ENGR241 staff, both team members who were new to SNF could get trained for all the fabrication tools needed for the process, and most of the characterization tools. We still need to finish trainings for FIB and AFM. As a result, we could re-design the process runsheet based on our knowledge, and ran through the fabrication steps. However, the failed characterization of both PGaN growth and PGaN etching failed us in such a way that all metal contacts were on top of PGaN. We will continue on this project as SNF community service project. This time we will follow more systematic ways of characterization.

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