# EE 412 report

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## Abstract

III-V integration on Si platforms provides many advantages including integrated multiple functionalities, simpler circuit design and scalability. However, the task of III-V integration on Si substrates remains a challenge due to the differences in lattice constants and crystal structures between III-V materials and Si. Many researchers have been studying different methods of III-V integration on Si, but most of them have issues of non-scalability or incompatibility with existing infrastructure. Rapid Melt Growth (RMG) is a promising III-V integration technique that provides significant advantages without the above-mentioned disadvantages. In this report, we describe the process developed in integrating InAs materials on Si substrate using RMG process. A FTIR measurement is used to measure the quality of InAs materials. Resistor structure and TLM structure were fabricated to study the electrical properties of the as grown materials.

## Background

Moore's law states that the number of transistors per square inch on integrated circuits doubles every year. The scaling of the transistors in semiconductor industry has been driven by Moore's law for five decades.

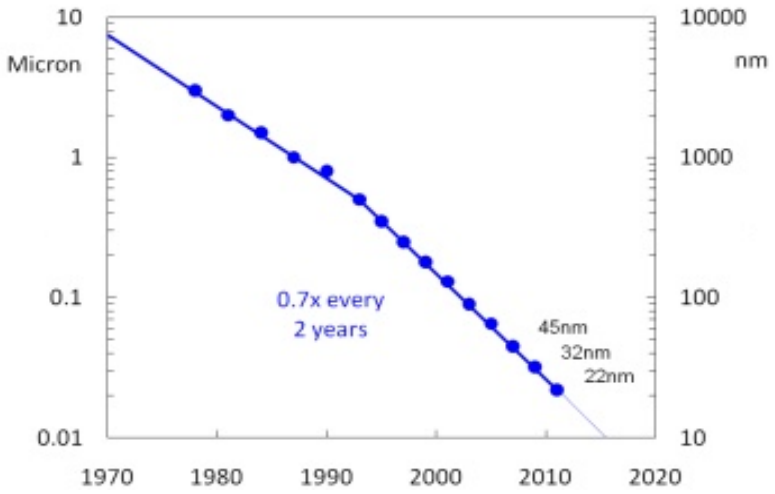



**Figure 1 Figure showing Moore's law**

However, the aggressive scaling of traditional silicon transistors is approaching their physical limits. Therefore, new materials with superior carrier transport properties are sought to extend the Moor's law scaling. Compound materials, among all the candidates for transistor materials, are the most promising candidate due to its high carrier mobility, its ability of integrating more functionalities like opt-electronics, RF circuit and MEMS etc, and the flexibility of band gap engineering. However, Compound materials are usually not compatible with silicon substrate and are traditionally fabricated separately on expensive compound substrates that are connected to the CMOS through external wiring. This increases the delay of the circuit and the cost. Therefore, finding a heterogeneous integration technology for those materials to be integrated on the silicon substrate is the key to next generation transistor technology.

Researchers have been actively looking for methods for III-V integration on silicon substrates. One method is the epitaxial growth of a heterogeneous material on Si through buffer layers that mitigates the strain and stress caused by the lattice

mismatch. The buffer layer usually requires high material usage and complex recipe optimization, which is not suitable for scalable production. Another method is wafer bonding, where III-V devices layers are grown on a suitable compound substrate and then transferred to the Si substrate. The size of the native compound substrate limits the scalability of this technique. Selective growth of material in opening trenches on Si substrate can be a good heterogeneous integration technique. However, because the materials are grown in trenches, the defects can grow out of the trenches, leaving behind the imperfect single crystal.

The Rapid Melt Growth (RMG), a method to liquid phase crystallize materials on silicon substrate, is easily manufactured, cost-effective and has high yield. It does not have the problems of the other above-mentioned technologies, making it one of the best candidates for the heterogeneous integration. The goal of this project is to integrate InAs on Si substrate using RMG method.

## Mechanism of RMG

The RMG technique is shown in the Figure 2 below. A single crystal substrate is used. A thin layer of dielectric layer is grown on the substrate and then patterned to open 4umx10um seed windows to the substrates. The target materials is then non-selectively grown on the patterned substrate and then patterned into 2μm×25μm stripes with one end in contact with the seed. A 1μm thick LPCVD $SiO_2$ layer is deposited on the whole structure. The structure is then put inside a standard rapid thermal annealing furnace under nitrogen ambient to be heated at a rate of $20^oC/s$ to ensure thermal equilibrium until the highest annealing temperature is reached. The highest annealing temperature is chosen to be at or

above the melting temperature of the target materials. Then the structure is cooled down with a cooling rate of 20°C/s. During cooling down, the molten materials start to crystallize from the end on the seed window and form single crystalline materials.

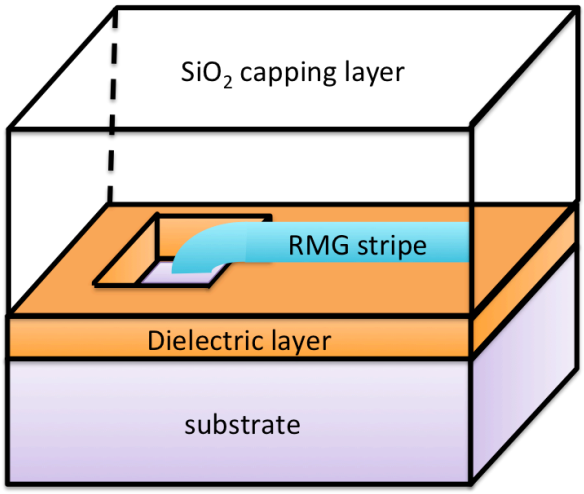



**Figure 2. Schematic of RMG stripes**

Although this method has been demonstrated to be effective for Ge and SiGe materials. It is not effective for III-V materials due to the eutectic point between Si and III-V. A typical phase diagram for a III-V and Si system is shown in Figure 3.

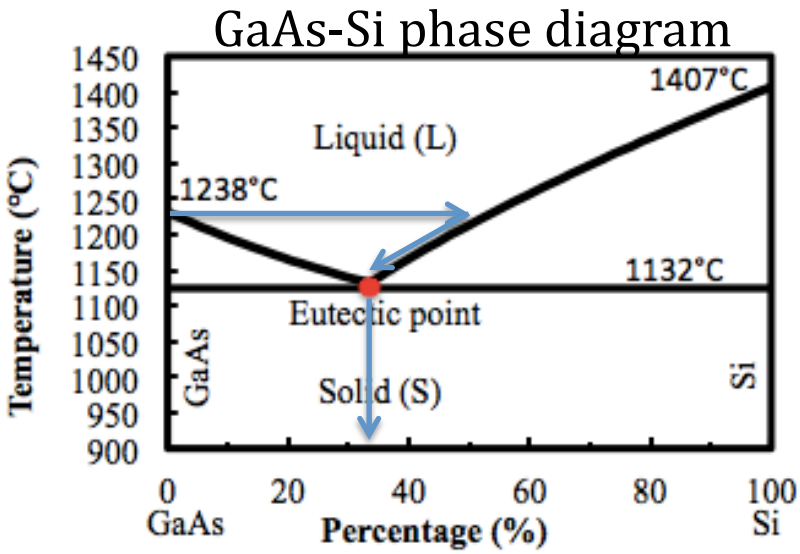



**Figure 3 GaAs-Si phase diagram**

It can be seen from the figure that the eutectic point is lower than the melting temperature of both materials. When the III-V is melted, it will start to melt Si until it reaches the liquidus line on the right. Once the crystallization starts, large amount of dissolved Si will segregate into Si islands due to the low solubility of Si in III-V in the solid state. SEM of InAs RMG on Si substrate after annealing is shown in Figure 4. The small dark region embedded in the InGaAs stripes is Si island. The cross section view at the seed region shows a pit inside the seed region which indicates significant Si melting.

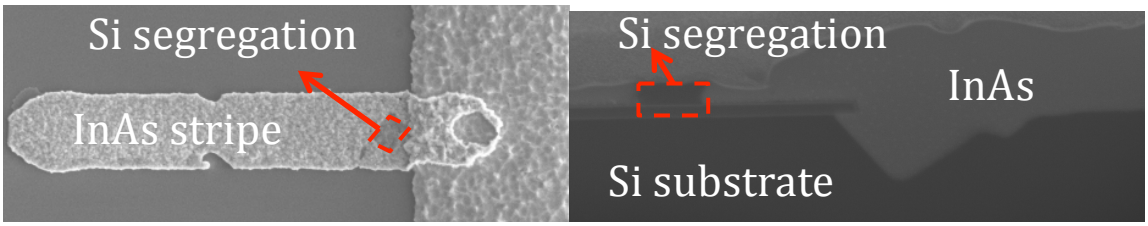



**Figure 4: Figures showing Si mixing with III-V. The left figure shows a Si island. The right figure is a cross section SEM image that shows a pit inside the Si substrate.**

## Experimental procedure and results

Si melting is a big problem if we were to integrate III-V on Si substrate through RMG method. Therefore a solution is proposed to prevent Si dissolution. In this project, we propose to insert an interfacial layer between Si and the target III-V to be grown. The purpose of the interfacial layer is to serve as the seed for the target III-V RMG and also barrier layer to stop Si from mixing with III-V.

GaAs has a zinc-blende crystal structure, which is very similar to the diamond structure of Si and have been well studied to be grown on Si substrate.

Its eutectic point with Si is much higher than the melting temperature of InAs, so it is a good candidate for the barrier layer. The epitaxial growth process of GaAs on Si

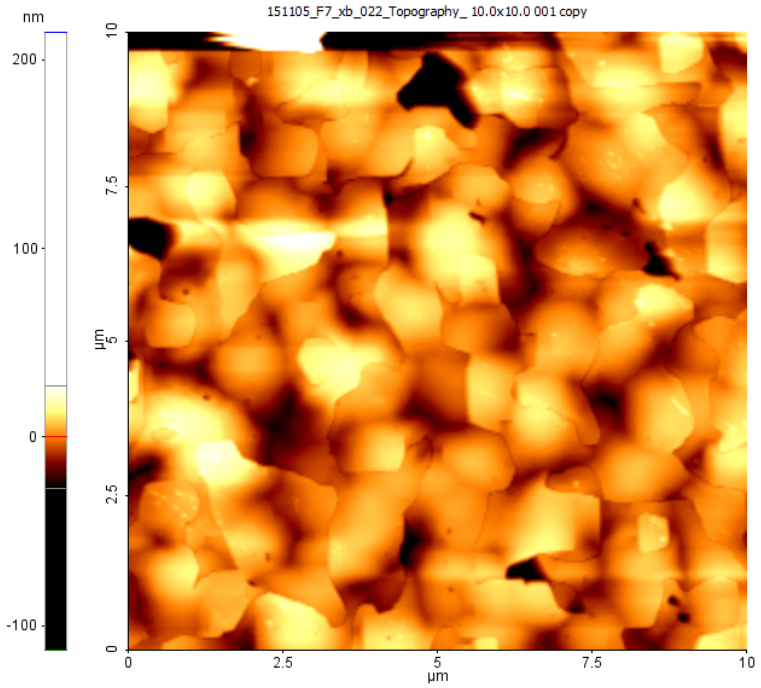
usually involves two steps growth: A Low temperature growth step to grow a buffer layer and a high temperature step to form a higher quality crystalline layer. The project will mainly focus on the optimization of this barrier layer using the MOCVD tool in SNF and some electrical measurements of this InAs RMG materials layer.

**GaAs epitaxial growth optimization**

It was found that Al atoms has a high sticking coefficient and thus can be used as a low temperature growth step. The initial growth recipe is a low temperature AlAs step at 425$^{o}$C for 15mins with V/III ratio of 24 followed by a high temperature GaAs step at 600$^{o}$C for 80mins with V/III ratio of 14. A few parameters are varied to find the optimum growth condition.

1. **Growth time variation**

The growth time was varied from 20mins to 80mins. The AFM images are shown below.



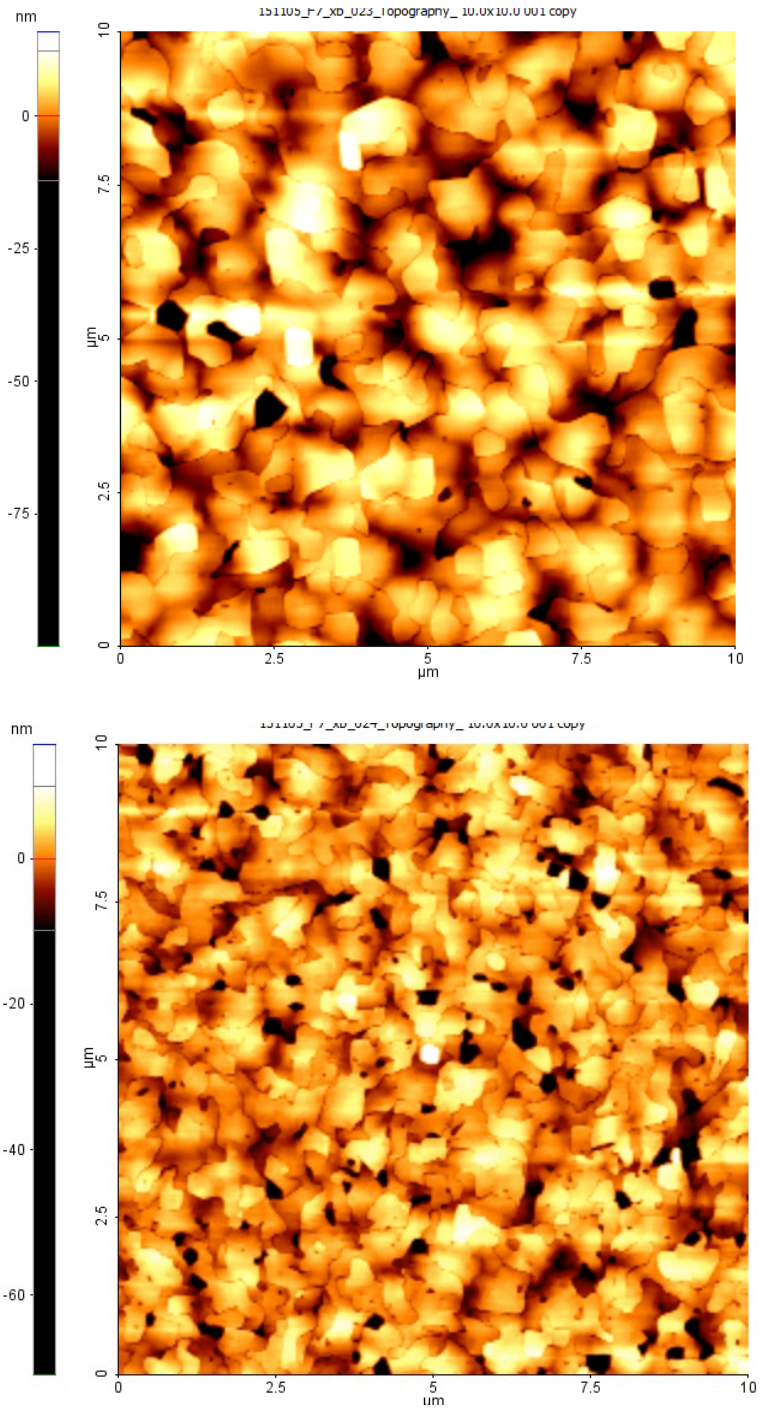



**Figure 5 AFM images showing different GaAs growth time. From top to bottom: 80mins GaAs growth time, 40mins GaAs growth time and 20mins growth time**

It can be seen that as the growth time increases, the grains in the GaAs layer becomes bigger, indicating coalescing of smaller islands to bigger islands. However,

the roughness and the peak-valley value indicate that the surface becomes rougher as the growth time increases from 20mins to 80mins.

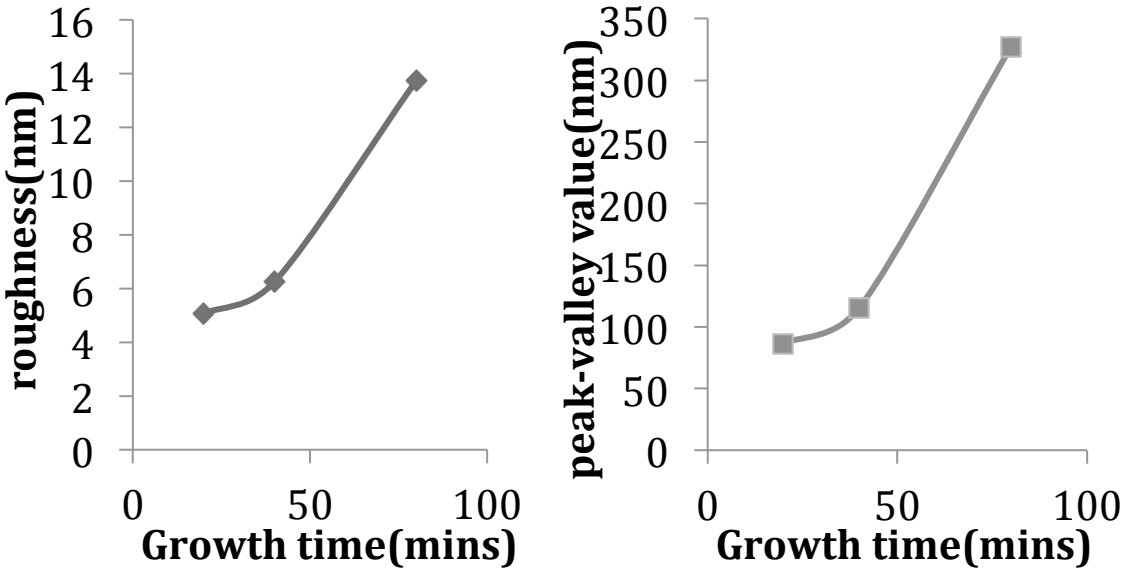



**Figure 6 Roughness and peak-valley value for different GaAs growth time**

**2. Inserting a high temperature AlAs growth step**

A high temperature AlAs layer is inserted between low temperature AlAs and high temperature GaAs layer in the hope of further improving the surface roughness. The growth is comprised of three steps: A low temperature AlAs growth step at 425$^{o}$C for 15mins with V/III ratio of 24, a high temperature AlAs growth step at 600$^{o}$C for 10mins with V/III ratio of 14 and a high temperature GaAs growth step at 600$^{o}$C for 10mins with V/III ratio of 14. The resulting AFM image are shown below. The peak-valley value is 154.934nm and the roughness is 17.349nm.

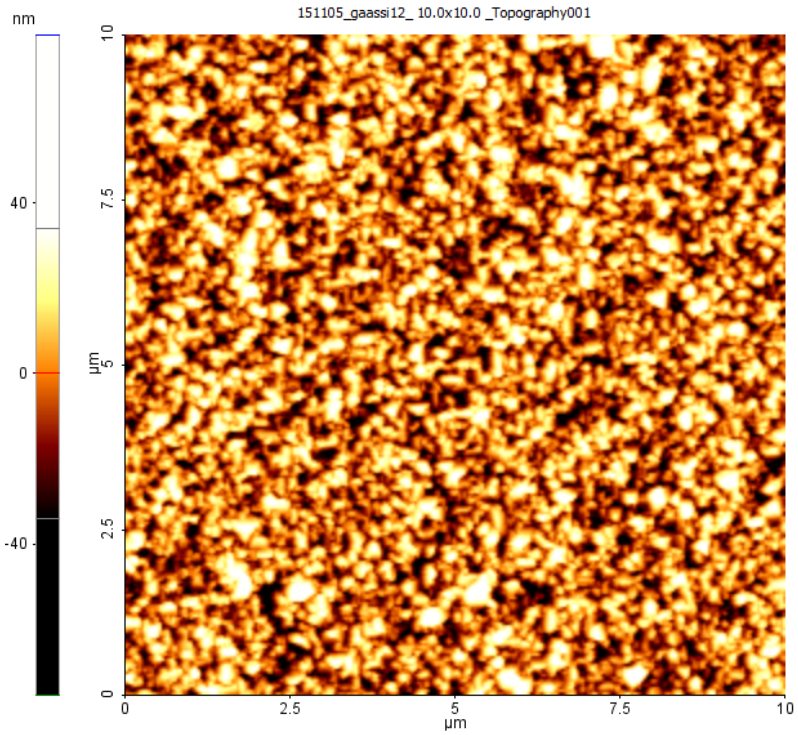
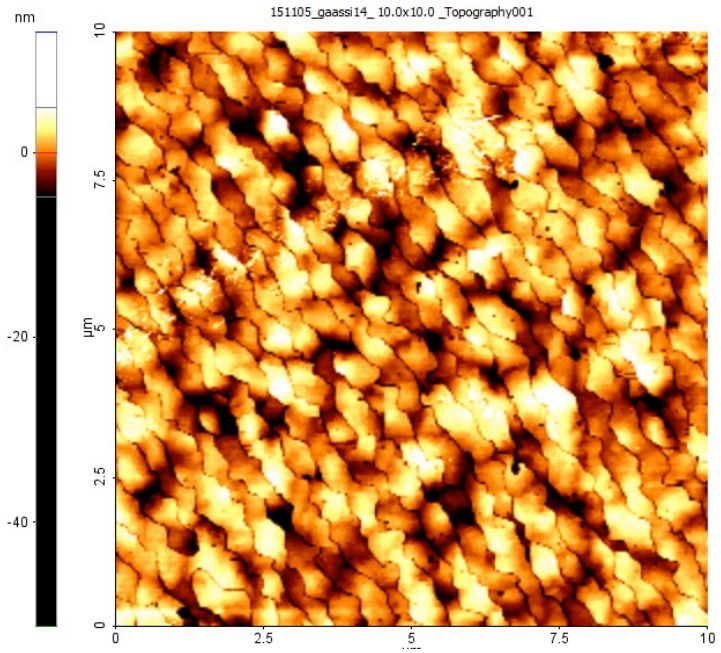



**Figure 7 AFM image of the three-step growth recipe.**

It can be seen that the resulting GaAs layer is much rougher and has much smaller grains. This could be due to the high sticking coefficient of the Al atoms. Al atoms do not have much mobility to move around and occupy the best lattice sites. As a result, the high temperature AlAs crystal is a less ordered crystal and has lots of crystal defects. Therefore a high temperature AlAs layer deposition is not recommended.

### 3. Variation of V/III ratio

The V/III ratio of the high temperature GaAs step is varied from 14 to 26. The AFM images are shown below.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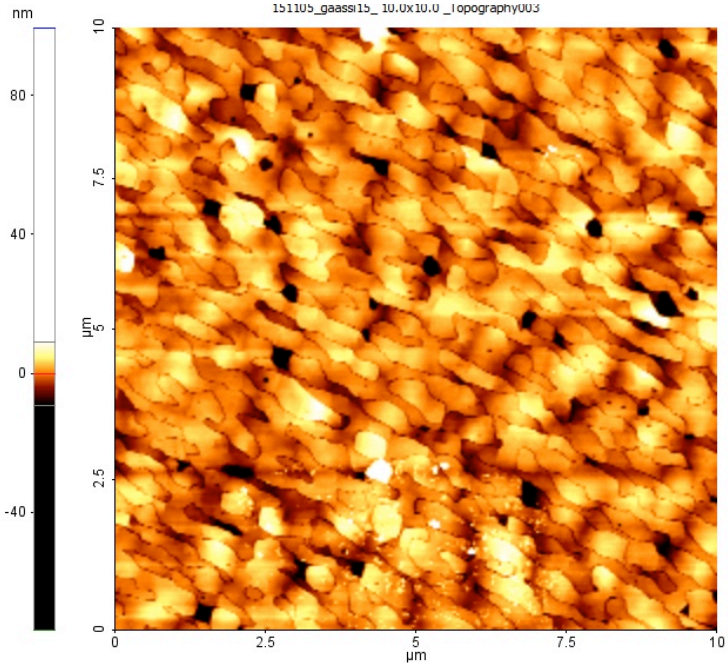
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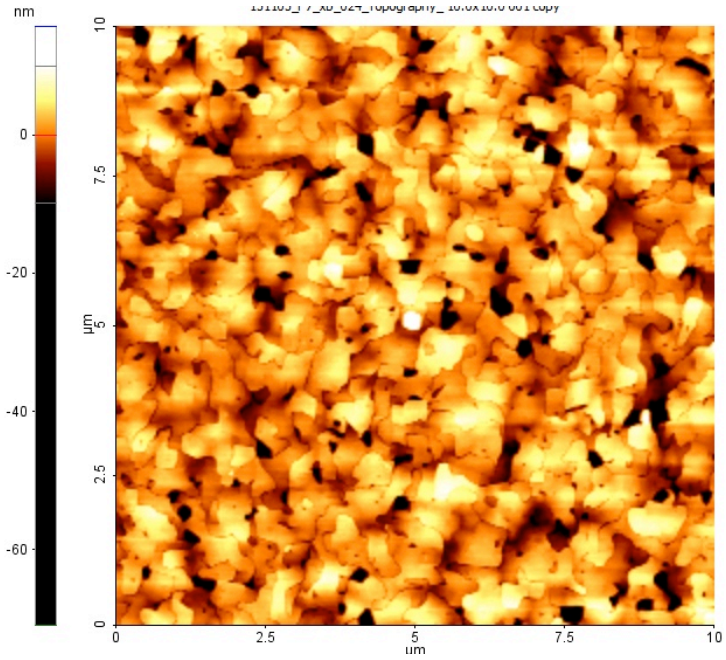



**Figure 8: AFM image showing different V/III ratio during GaAs growth. From top to bottom: V/III ratio of 14, V/III ratio of 20 and V/III ratio of 26.**

As the V/III ratio increases from 14 to 20, the morphology changes from jigsaw puzzle shaped grains to elongated grains aligned in (111) direction and the roughness decreases. Further increasing the V/III ratio, however, increases the surface roughness and shortens the aligned grains.

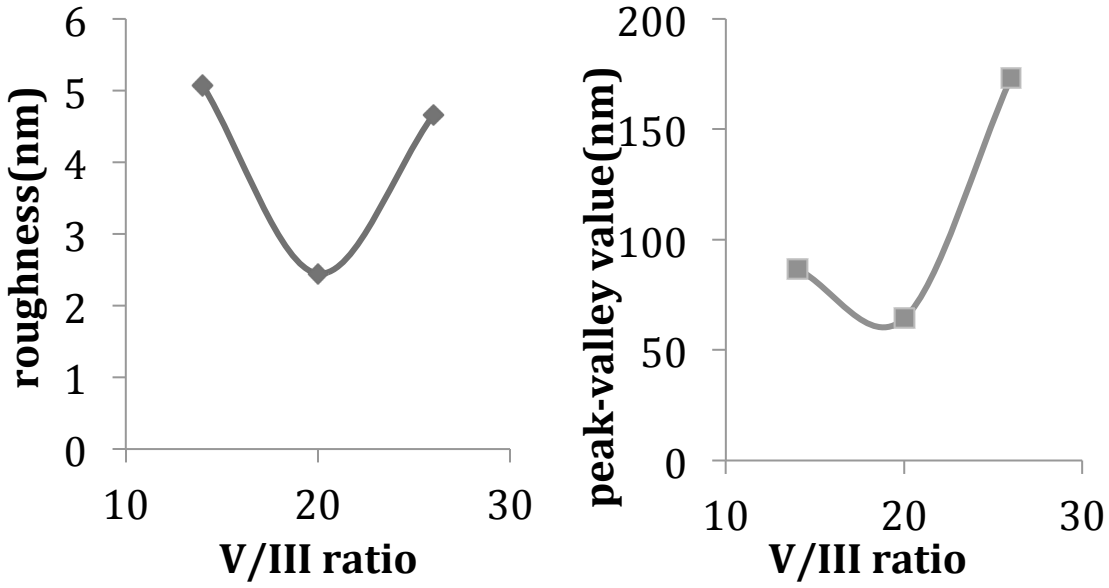


**Figure 9 Surface roughness and peak-valley value for different V/III ratio**

Therefore the optimum growth recipe is determined to be a two-step growth recipe: A low temperature AlAs growth step at 425$^{o}$C for 15mins with V/III ratio of 24 followed by a high temperature GaAs growth step at 600$^{o}$C for 20mins with V/III ratio of 20.

**Optical and Electrical measurements of InAs RMG materials**

After the InAs RMG fabrication on the GaAs barrier, a FTIR transmission measurement was done on the sample. The FTIR measurement shows a dip at the 0.35eV, indicating a successful growth of InAs semiconductor materials.

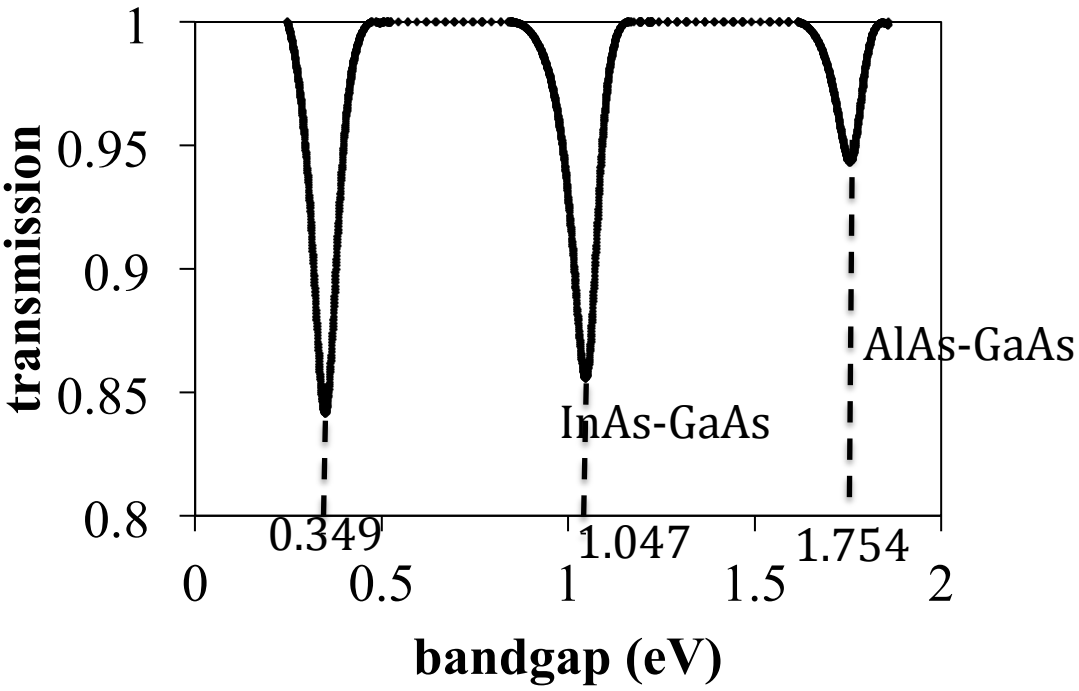



**Figure 10 FTIR measurements**

Two terminal resistor structures were fabricated to measure the resistance of the as grown InAs materials. After the rapid thermal annealing, the 1um $SiO_2$ capping layer was then selectively removed by either dry $SiO_2$ etching or wet HF

etching. Then 200nm LOL2000 was spin on the surface followed by a 1um 3612 photoresist coating. The LOL2000 was used because it can be undercut by the developer and makes the lift-off process easier. A photolithography exposure was done on the coated samples for 2s and the patterns were developed in the MF-26A for 45s. It was found that no post-exposure baking was better for developing the metal pad patterns. The metal film was then deposited on the sample surface using e-beam evaporation tool. The contact was composed of 10nm Ti and 90nm Ni. The lift-off process was then done in acetone liquid overnight to form the contact pads. At last, 1165 was used to remove all the residue lol2000.

During the process, it was found that while etching away the $SiO_2$ capping layer, the underlying $SiO_2$ layer was also over etched, exposing the substrate, which provides a leakage way for the current and affect the final I-V results. Therefore a new underlying dielectric structure was developed as shown in Figure 11.

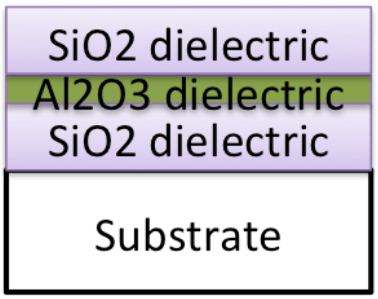



**Figure 11 New dielectric structure for making devices**

The new dielectric structure is composed of a 30nm $SiO_2$ film followed by 10nm $Al_2O_3$ film and than another 30nm $SiO_2$ film. The bottom 30nm $SiO_2$ layer provides sufficient electrical isolation while the $Al_2O_3$ layer acts as an etch stop layer because annealed ALD $Al_2O_3$ film is known to be resistant to HF etch. After the de-

capping process, the substrate was unexposed, proving the structure was effective. Metal pads were then fabricated on the substrate. The I-V curve measurements for a device with contact spacing of 6um were shown in Figure 12. The results were compared to the amorphous InAs materials and the single crystalline InAs substrates.

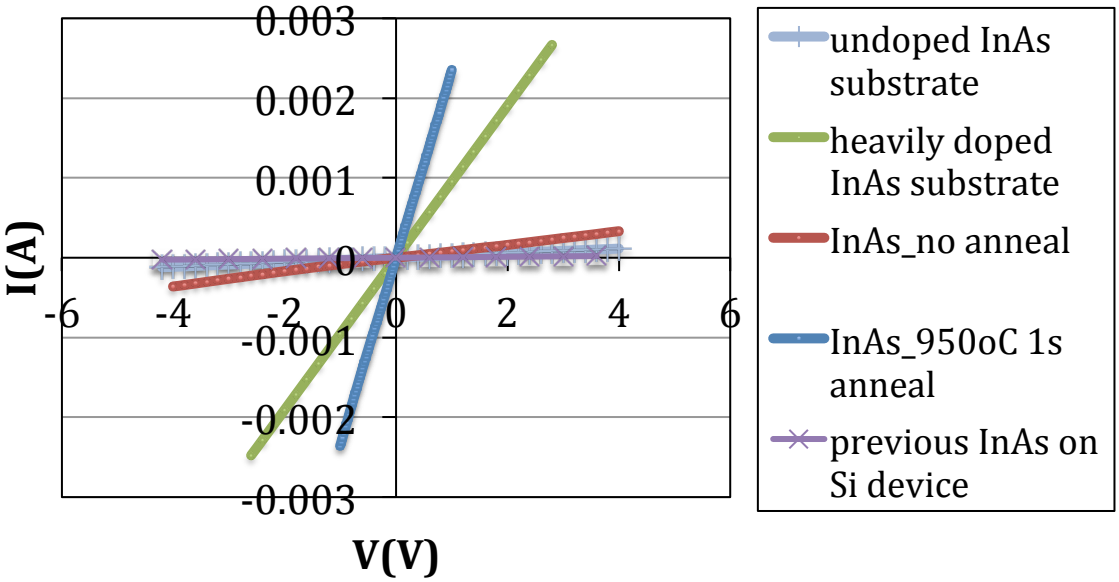



**Figure 12 Comparison of I-V curves between InAs RMG materials and several InAs substrate**

It can be seen that the amorphous as-deposit InAs has the similar resistance to the un-doped InAs substrate in the market whereas the annealed sample has a much lower resistance than the heavily doped InAs substrate. The I-V curve shows a straight line, which means good ohmic contact. A transmission line measurement structure is fabricated to find the resistivity and contact resistance for the InAs device. The TLM results are shown in Figure 13.

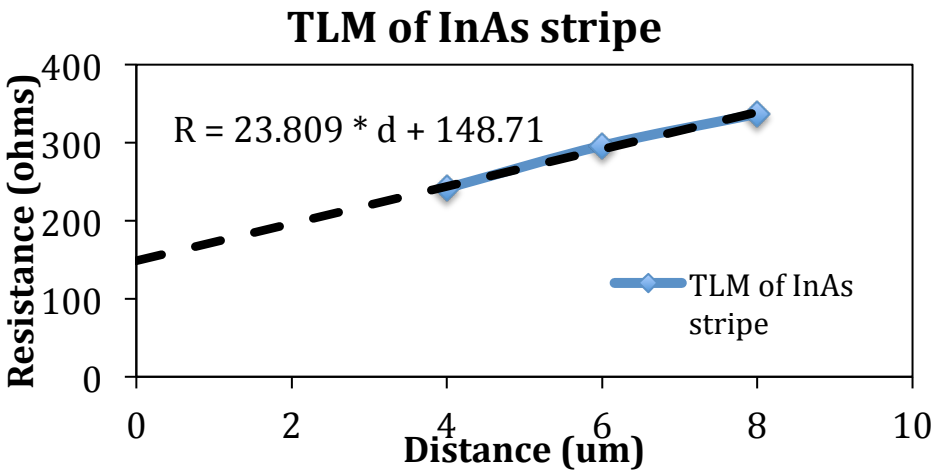



**Figure 13 TLM results of the as grown InAs RMG materials**

The contact resistance between the InAs materials and Ni metal is calculated to be 2.9742E-06 Ω•cm$^2$. The resistivity of the InAs is calculated to be 4.76E-4 Ω•cm. The contact resistance is shown to be similar to the literature value and the resistivity is shown to be 100 times higher than the un-doped InAs substrate and 5 times higher than a heavily doped inAs substrate. The low resistivity can be attributed to the non-stoichiometry inside the InAs film.

Auger Electron Spectroscopy was used to determine the elemental composition of the as grown InAs stripes. 10 positions on the stripe were measured as shown in the SEM image below.

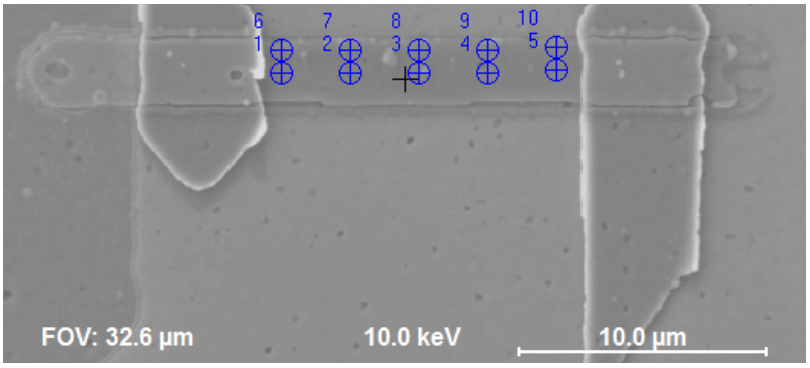


**Figure 14 SEM image showing the position of the data points**

Depth profiles were measured for each one of the positions. The elemental concentration from position 6 to position 10 on the stripe surface is shown below

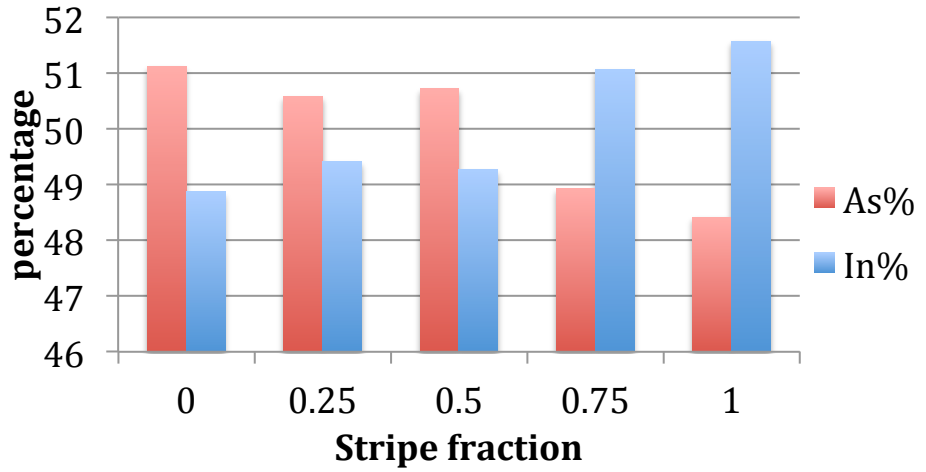
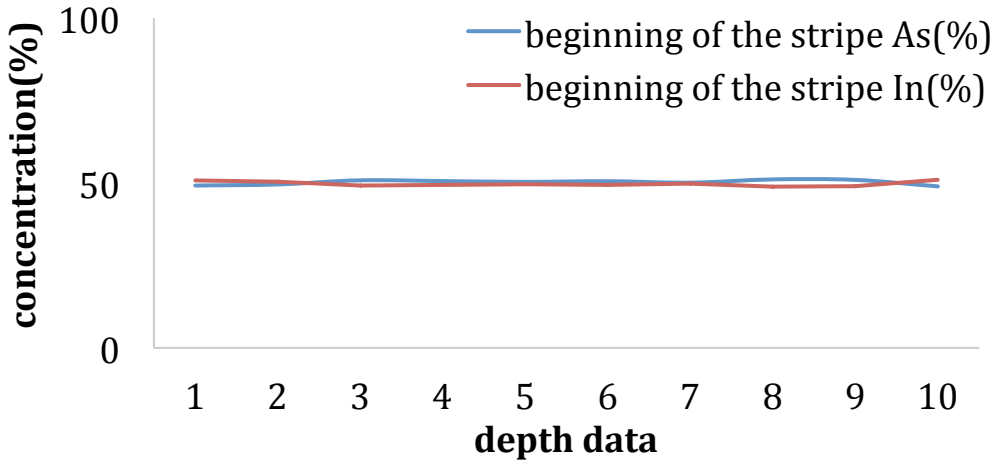



**Figure 15 AES measurements showing In & As concentration for from point 6 to point 10**

As we move away from the stripe head, the Indium concentration starts to increase while the As concentration starts to decrease. The non-stoichiometry can lead to atoms occupying the wrong lattice sites and leads to self-doping. The depth profile of the position 1 and position 5 are shown in Figure 16. It can be seen that the concentration of In and As are consistent throughout the depth of the stripe.



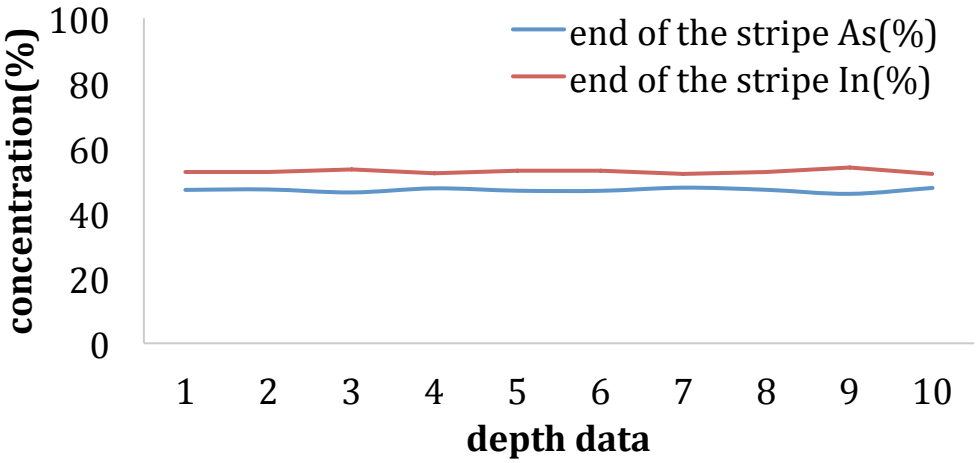



**Figure 16 Depth profiles of point 1 and point 5. From top to bottom: depth profile for point 1, depth profile for point 5**

A more optimized growth recipe for InAs can restore the stoichiometry and leads to lower doped InAs RMG materials.

## Conclusion

In this project, we proposed a way to mitigate Si mxing inside III-V materials during RMG process. We optimized the GaAs growth recipe on Si substrate and measured the electrical properties of the as-grown InAs RMG materials. It was found that the grown InAs has low resistivity. A non-stoichiometry can be used to explain the unusual low resistivity. Future work includes MOSFET fabrication and stoichiometric InAs film deposition.

## Acknowledgement

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