Variable Trench Optimization for DRIE of SOI in PT-DSE

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Abstract

This work seeks to add the PlasmaTherm Deep Silicon Etcher (PT-DSE) tool as a candidate for etching of Silicon-on-Insulator (SOI) wafers at the SNF. Currently, the only tool capable of performing this kind of etch at the SNF is the STS2. This tool has been down for maintenance for a considerable time and groups have begun to outsource their work for this etching step. We have developed a recipe for variable, high aspect ratio features with good etch profile characteristics. We have also investigated oxide charging issues with the PT-DSE tool and provide insight to the resolution of the issue.

Background

Deep Reactive Ion Etching (DRIE) of SOI wafers to the buried oxide (BOX) layer is a common technique used in MEMS technology. This characteristic etch has traditionally been performed on Surface Technology Systems' DRIE tool at the SNF (STS2). STS2 has given superior performance for etching various trench widths for multiple device layer thicknesses yielding exceptionally smooth sidewalls with minimal blowout and footing. However, the tool has proven difficult to maintain and has logged much downtime. The objective for this project is to include the PT-DSE etcher at SNF as a potential tool to perform this critical step. PT-DSE is a 3rd generation plasma etcher with a much better maintenance record than the previous generation STS tool. Unfortunately, the PT-DSE has proven to be difficult to use with SOI wafers. Particular issues arise with the tools mask selectivity and extreme notching at the Silicon-insulator interface. Previous work has been conducted to minimize the notching effect for this particular tool by the PlasmaTherm group themselves [1]. However, this work reported good results only for aspect ratios smaller than 22:1. The goal of this project is to develop a standard recipe that can etch trenches with widths ranging from 0.7 to 1.5 μm down to the oxide insulation of 20 and 40 μm device layer SOIs with minimal blowout and notching.

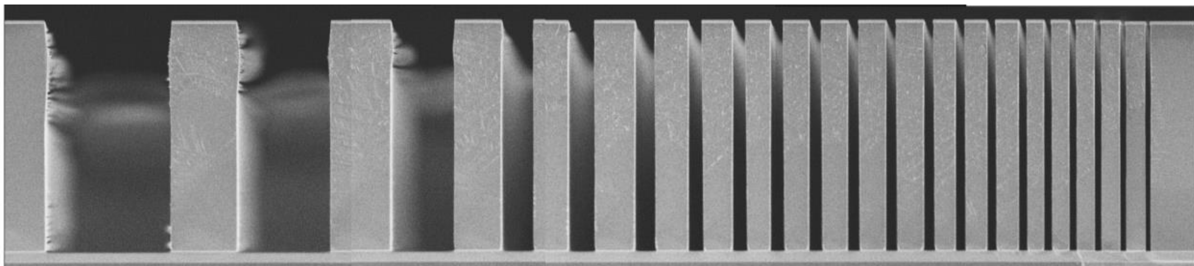


***Figure 1**: Target profiles for a 20 μm device layer (trenches 20 to 0.5 μm left to right). Reference fabricated using STS Pegasus at University of Michigan.*

Experimental Method

The primary objective of this work was to minimize notching for high aspect ratio trenches on SOI wafers. However, this would require a large quantity of SOI wafers for recipe development, which was beyond our budget and existing resources. One potential solution would be to use pieces of SOI wafer, instead of the wafer in its entirety, to perform the characterization. This technique may not be ideal, however, as the processes may be very different between pieces and full wafers. Differences in thermal and electrical properties between pieces and whole wafers, such as thermal dissipation, would likely have an impact. A better solution, and our implemented methodology, is to use thick epitaxial poly-Si on oxide. Our experimental method consisted of two phases. First, single crystal silicon wafers were used to optimize the desired etch properties of the bulk silicon. Blowout, scalloping, tapering, and the aspect ratio dependence of the trench depth to the trench width, or simply ARD, were to be minimized. After obtaining the optimized etch profile, poly-Si on oxide wafers were fabricated to minimize notching, while maintaining the sidewall profiles found in the previous step.

Mask Design

The test wafers were placed in a thermal oxidation chamber to grow a 1μm oxide hard mask. The mask shown in Figure 2 was obtained and used to pattern a 1 μm thick layer of SPR955 positive photoresist atop the hard mask. The photoresist was exposed and developed, and the wafers were etched in an oxide plasma etching chamber. Trench geometries ranging from 0.4 to 1.5 μm in width were defined in the oxide and photoresist layers as shown in Figure 2.

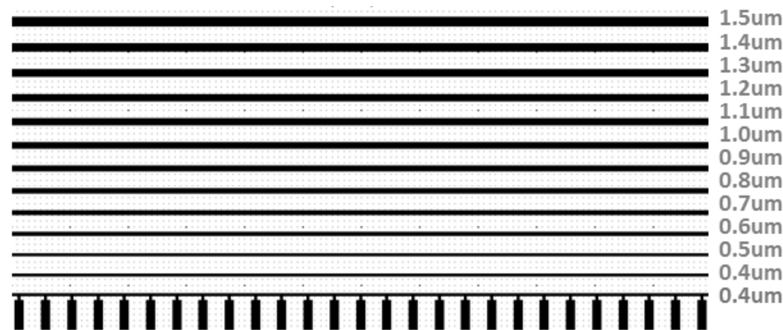


Figure 2*: Mask design for etch test structures. Trench widths range from 0.4μm to 1.5μm.*

Bulk Etch Optimization

A starting recipe for PT-DSE had to be chosen to begin the optimization. Ideally, the starting recipe should be close to the desired result so that optimization may be performed with confidence. Therefore, we first investigated using PT-Smooth, a previously optimized recipe for PT-DSE, as our starting recipe. PT-Smooth was a recipe developed to minimize scalloping for the DRIE tool [2]. Figure 3 shows that this recipe works well for specific trench widths of 1 μm down to a depth less than 10 μm. However, performing this etch for deeper trenches proved to be a challenge for this recipe. It was found that PT-Smooth tapers significantly and the etching becomes self-limiting. Grassing was also observed for larger trenches. It was determined that PT-Smooth was a poor candidate for the purposes of this project.

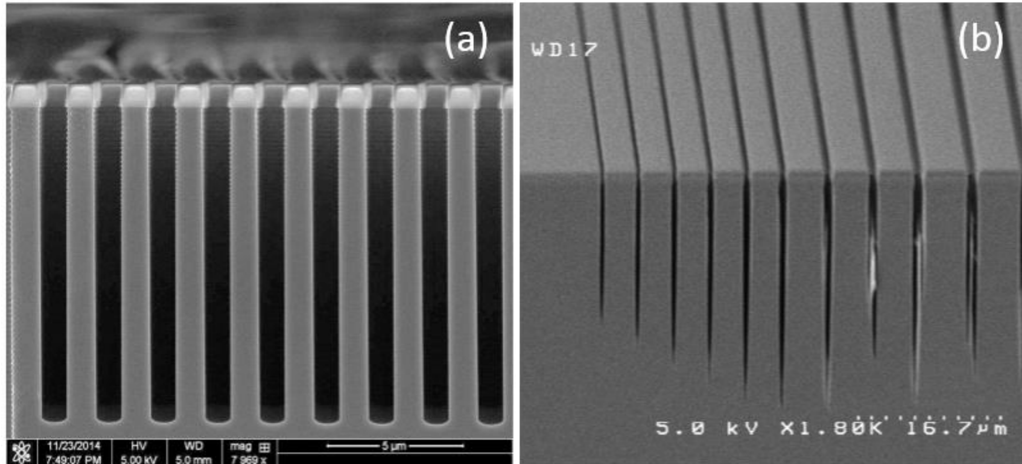


Figure 3*: PT-Smooth etch characteristics. (a) 1 μm trenches etched ~9 μm deep [2]. (b) 0.4μm to 1.5μm trenches attempted to 20 μm depth.*

Another recipe was investigated as a potential candidate for our starting recipe. This recipe was based on the standard DSE-FAT recipe and was provided by a fellow lab member. The recipe performed much better at etching variable trench widths to appreciable depths, as seen in Figure 4. However, the observed blowout and tapering were found to be an issue.

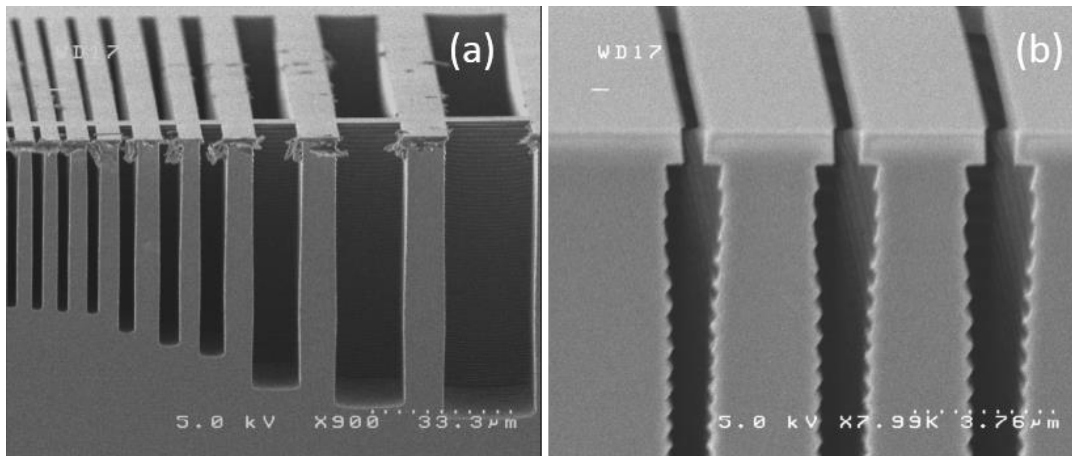


Figure 4: *Potential starting recipe investigated for variable trench optimization.*

To combine the advantages of both recipes, we introduce a two pass etch system. The first pass, which is similar to PT-Smooth, provides a gentle etch to reduce the blowout under the hard mask. The second pass then provides a faster etch with etch time morphing to minimize tapering while maintaining good bulk etch characteristics for variable, high aspect ratio trenches. Our recipe was finalized through iteration and knowledge of etch characteristic dependencies of tool parameters shown in Figure 5.

Variable Increased	Etch Rate	Sidewall Roughness	Feature Blowout	Grass	Photoresist Selectivity	Polymer Breakdown
Etch gas	↑	↑	↑	↓	↑	↑
Dep gas	↓	↓	↔	↑	↑	↓
Etch:Dep time ratio	↑	↑	↑	↓	↔	↔
Pressure	↑	↑	↑	↓	↑	↑
Etch coil power	↑	↑	↑	↓	↑	↑
Dep coil power	↓	↓	↓	↑	↔	↓
Platen power	↔	↔	↔	↓	↓	↔
Etch EM1 value	↓	↔	↓	↔	↑	↓
Etch EM1 delay time	↔	↔	↔	↓	↓	↔

Figure 5*: STS2 etch characteristics matrix from SNF wiki.*

The results from the iterative process are shown in Figure 6. It can be seen that the etch blowout was significantly reduced using this method.

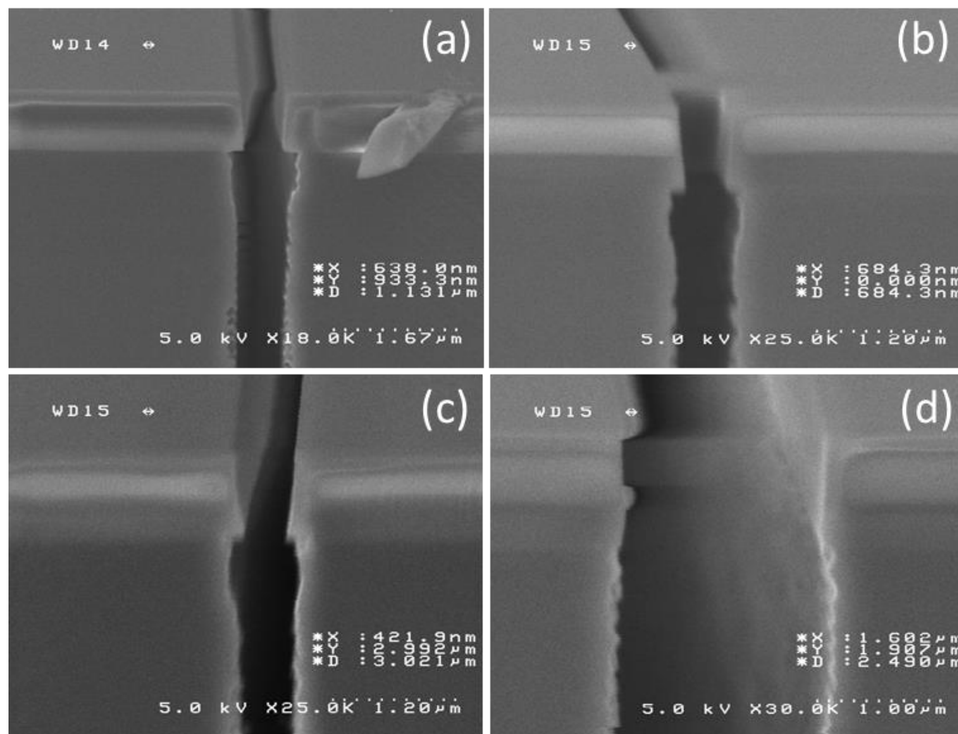


Figure 6: *Starting recipe development process for variable trench optimization in PT-DSE. (a) First iteration. (b) Second iteration. (c) Third iteration. (d) Fourth iteration.*

The finalized starting recipe was found to have acceptable etch characteristics for optimization of the bulk etch profile. Figure 7 shows the family of trenches etched. The transition from the slow etch used to minimize blowout to the aggressive etch used to reach depths required for our high aspect ratio requirements may also be seen. We find we still have good depth etches for many trench widths.

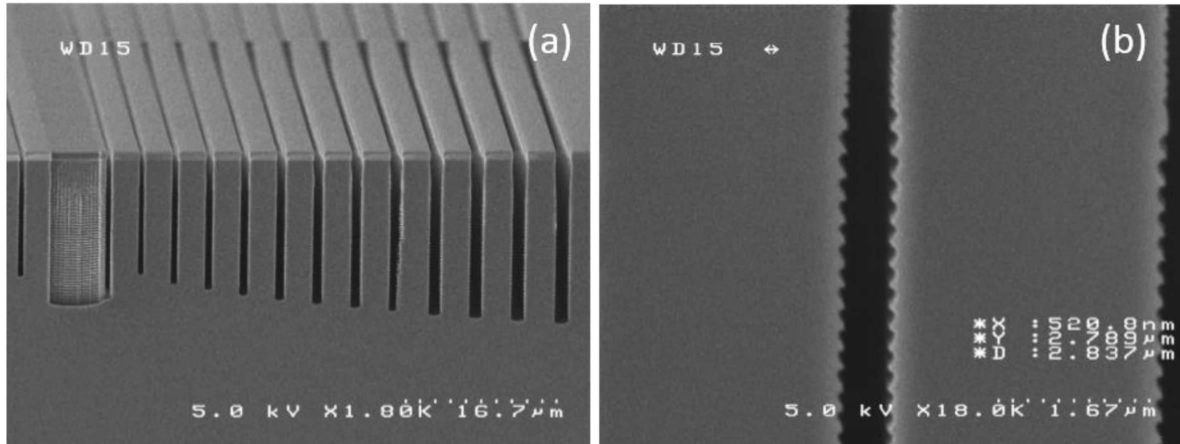


Figure 7: *Starting recipe developed for variable trench optimization in PT-DSE. (a) 0.4 to 1.5 µm width trenches etched to ~20 µm depth. (b) Close up of transition from first pass to second pass.*

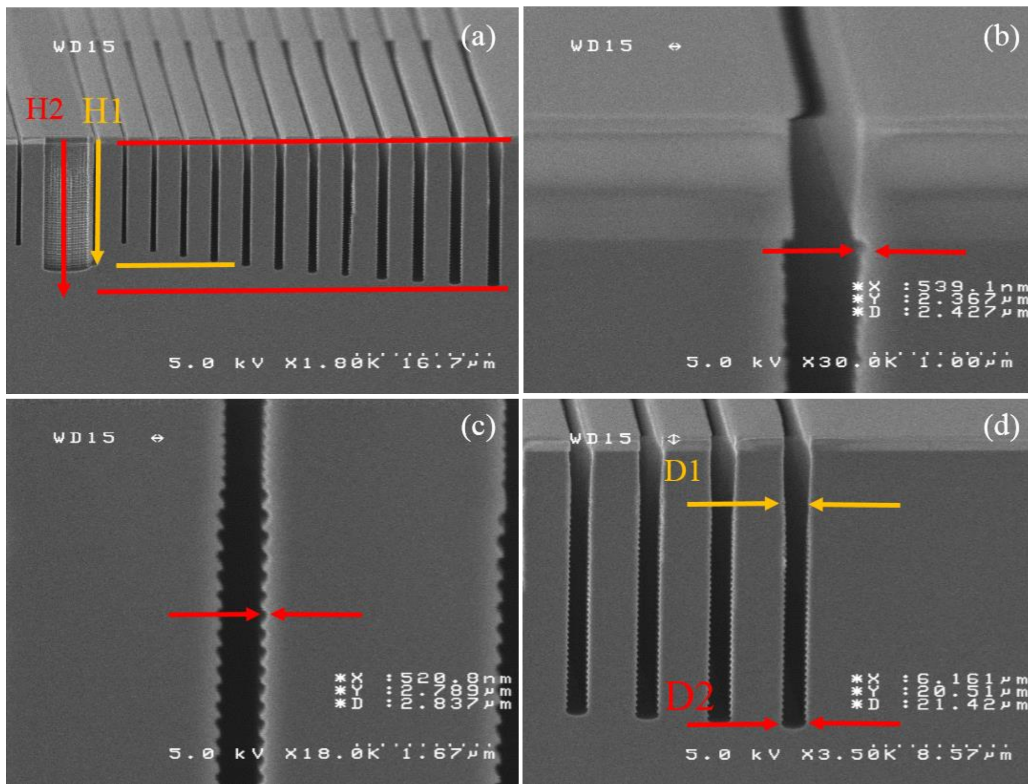
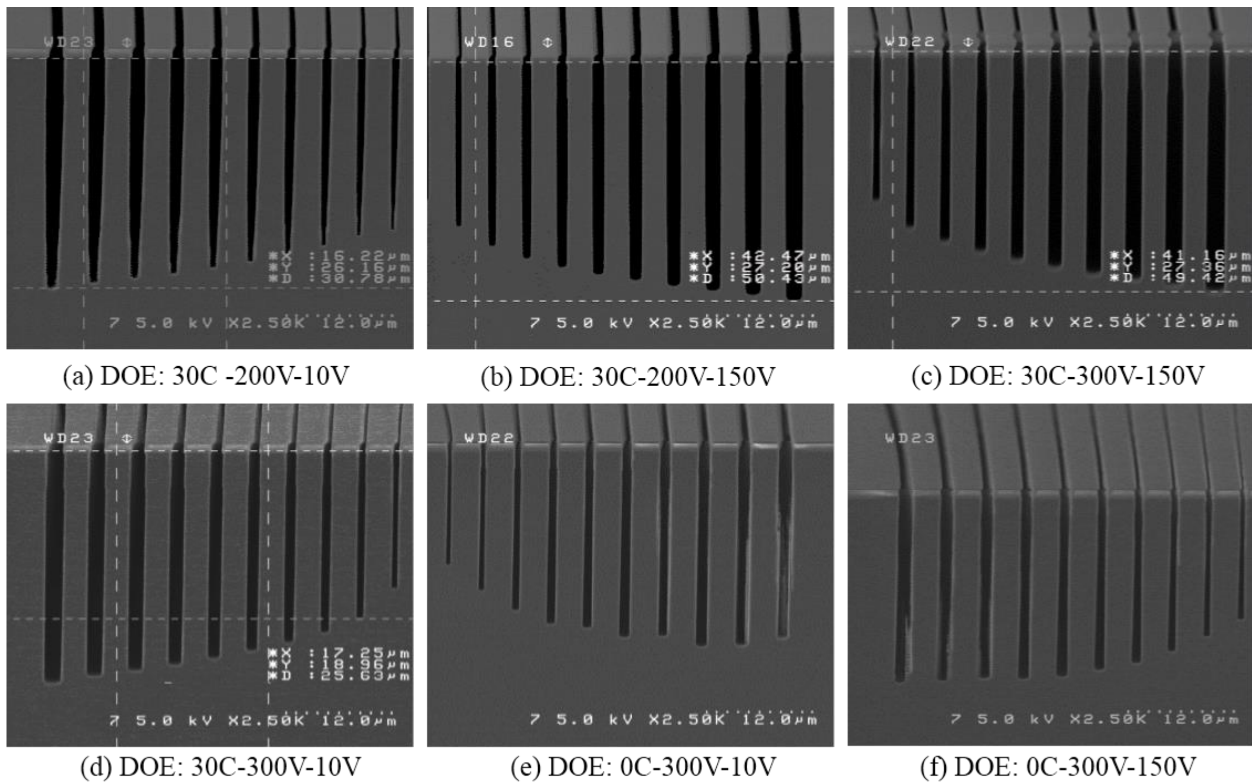


Figure 8: *Etch characteristics for optimization: (a) Aspect ratio dependence (ARD). (b) Blowout. (c) Scalloping. (d) Tapering.*

Bulk etch optimization was proceeded after obtaining the finalized starting recipe. The characteristics of interest in this study were aspect ratio dependence of the trench depth (ARD), blowout, scalloping, and tapering. Each characteristic is shown in Figure 8.

JMP analysis was performed to optimize the etch characteristics. The Design of Experiment (DOE) and results are shown in Figure 9 and Table 1, respectively. A full analysis was found difficult to perform due to the appearance of complex issues such as grassing during the analysis. Therefore, the results of the experiment were used as a screening DOE to find the optimization region. Table 1 shows the optimization region highlighted in red. The previous iterative method was then performed to achieve the final recipe.



(a) DOE: 30C -200V-10V (b) DOE: 30C-200V-150V (c) DOE: 30C-300V-150V

(d) DOE: 30C-300V-10V (e) DOE: 0C-300V-10V (f) DOE: 0C-300V-150V

Figure 9: *SEM pictures showing the DOE results*

Table 1: *Summary of etch characteristics of DOE results*

	Pattern	Temp	EtchA	EtchB	ARD	Blowout	Scalloping	Taper
1	"+--"	30	200	10	1.30	252	111	1.32
2	"-++"	0	300	150		Grass!!!		
3	"-+-"	0	300	10	N/A	50	N/A	N/A
4	"+-+"	30	200	150	1.33	202.9	62.5	1.06
5	"++-"	30	300	10	1.39	128.9	128.9	1.12
6	"--+"	0	200	150		Grass!!!		
7	"+++"	30	300	150	1.37	134	134	1.06
8	"---"	0	200	10		Grass!!!		

Table 2 shows the resulting optimized recipe for 20 µm deep trenches. An optimized recipe for 40 µm deep trenches was also developed by increasing the number of cycles for the 2nd pass as well as increasing the etch ramping to prevent tapering (Table 3).

Table 2: *Optimized variable trench width recipe for 20 µm*

Loop 1 – No. of cycles = 20

Parameter	Dep	Etch A	Etch B
C4F8 sccm	150	to pump	to pump
SF6 sccm	*150 to pump*	150	30
Ar sccm	30	30	30
Pressure	30	35	40
ICP watts	1500	1500	1500
V p-p	10	250	10
waveform	1	1	1
Step time (s)	1.5	1	1

Loop 2 – No. of cycles = 60

Parameter	Dep	Etch A	Etch B
C4F8 sccm	150	to pump	to pump
SF6 sccm	*150 to pump*	150	250
Ar sccm	30	30	30
Pressure	25	40	50
ICP watts	2000	2000	2000
V p-p	10	250	100
waveform	1	1	1
Step time (s)	2.3	1	1.5 to 2.25

Table 3: *Optimized variable trench width recipe for 40 µm*

Loop 1 – No. of cycles = 20

Parameter	Dep	Etch A	Etch B
C4F8 sccm	150	to pump	to pump
SF6 sccm	*150 to pump*	150	30
Ar sccm	30	30	30
Pressure	30	35	40
ICP watts	1500	1500	1500
V p-p	10	250	10
waveform	1	1	1
Step time (s)	1.5	1	1

Loop 2 – No. of cycles = 120

Parameter	Dep	Etch A	Etch B
C4F8 sccm	150	to pump	to pump
SF6 sccm	*150 to pump*	150	250
Ar sccm	30	30	30
Pressure	25	40	50
ICP watts	2000	2000	2000
V p-p	10	250	100
waveform	1	1	1
Step time (s)	2.3	1	1.5 to 3

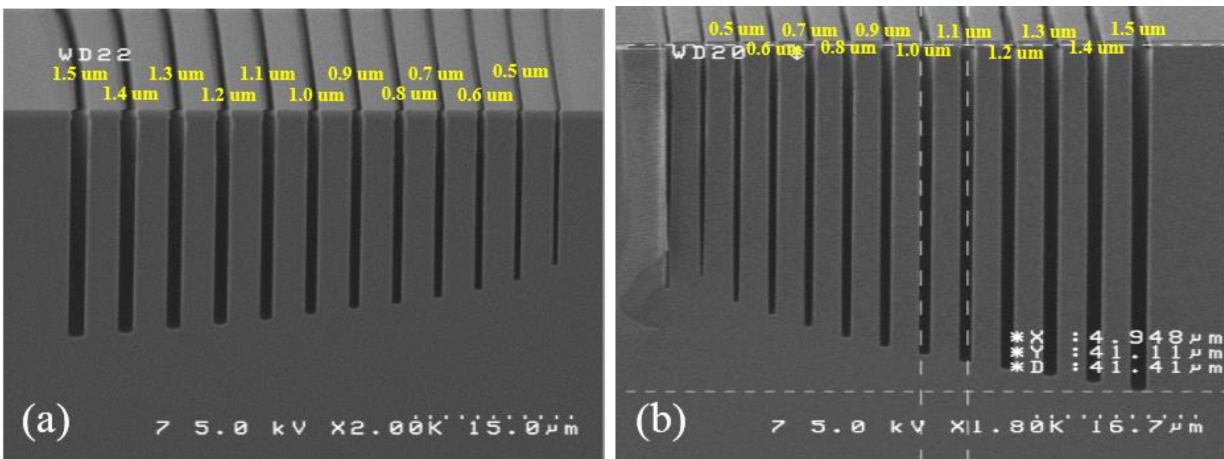


Figure 10: *SEM images of optimized etch profiles for variable trench widths. (a) 20 µm depth. (b) 40 µm depth.*

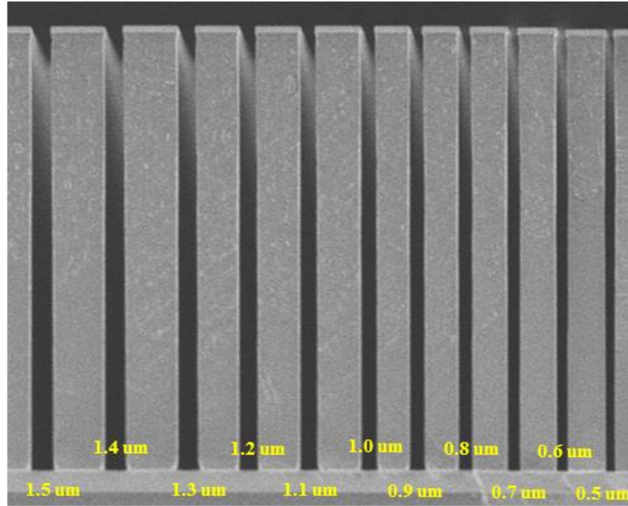


Figure 11: *Reference etch from STS Pegasus at University of Michigan*

Table 4: *Comparison between PT-DSE optimized recipes at SNF and STS Pegasus recipe at Michigan.*

	Depth	ARD	Blowout (nm)	Scalloping (nm)	Taper
Stanford	20um	1.23	169.0	< 100	1.03
	40um	1.23	168.6	107.0	1.10
Michigan	Depth	ARD	Blowout (nm)	Scalloping (nm)	Taper
	40um	N/A	150.0	< 100	1.15

Figure 10 shows the SEM images of the optimized etch profiles. Figure 11 shows the SEM image of the reference etch profile from STS Pegasus at the University of Michigan. We find that the recipes are highly comparable. Table 4 shows the comparison between the etch characteristics of interest between the recipes optimized for PT-DSE and the reference generated at the University of Michigan. We now have optimized bulk etch recipes for both 20µm and 40µm deep trenches.

SOI Etch Optimization

Optimization of the SOI etch was performed once a suitable bulk etch had been developed. The previous two pass system was used in addition to a third pass which was designed by the PlasmaTherm tool manufacturer to reduce oxide charging, which leads to the notching phenomenon. The recipe we used for testing SOI etching is detailed in Table 5. Waveform 3 was used for the third pass to provide pulsing of the bias voltage with 15% on time. It has been reported that pulsing of bias voltage reduces the notching effect when etching SOI wafers [3, 4].

Table 5: *SOI etching recipe used for PT-DSE.*

Loop 1 – No. of cycles = 20

Parameter	Dep	Etch A	Etch B
C4F8 sccm	150	to pump	to pump
SF6 sccm	*150 to pump*	150	30
Ar sccm	30	30	30
Pressure	30	35	40
ICP watts	1500	1500	1500
V p-p	10	250	10
waveform	1	1	1
Step time (s)	1.5	1	1

Loop 2 – No. of cycles = 34

Parameter	Dep	Etch A	Etch B
C4F8 sccm	150	to pump	to pump
SF6 sccm	*150 to pump*	150	250
Ar sccm	30	30	30
Pressure	25	40	60
ICP watts	2000	2000	2000
V p-p	10	250	100
waveform	1	1	1
Step time (s)	2.3	1	1.5 to 4

Loop 3 – No. of cycles = 90

Parameter	Dep	Etch A	Etch B
C4F8 sccm	125	15	15
SF6 sccm	*75 to pump*	75	100
Ar sccm	30	30	30
Pressure	20	20	20
ICP watts	1600	1250	1250
V p-p	10	400	215
waveform	3	3	3
Step time (s)	2	2	1.5

In lieu of SOI wafers which are costly, Polysilicon on oxide wafers were fabricated according to the process described in Figure 13. First, a 1 µm oxide layer was thermally grown using the Thermco tool at the SNF. Next, 20 µm of polysilicon was deposited using the epitaxial silicon reactor. Chemical-mechanical polishing (CMP) was performed to smooth out the wafer surfaces. A 1 µm oxide hard mask was then grown followed by lithographic patterning and etching of the hard mask. Finally, the test structures were etched using PT-DSE.

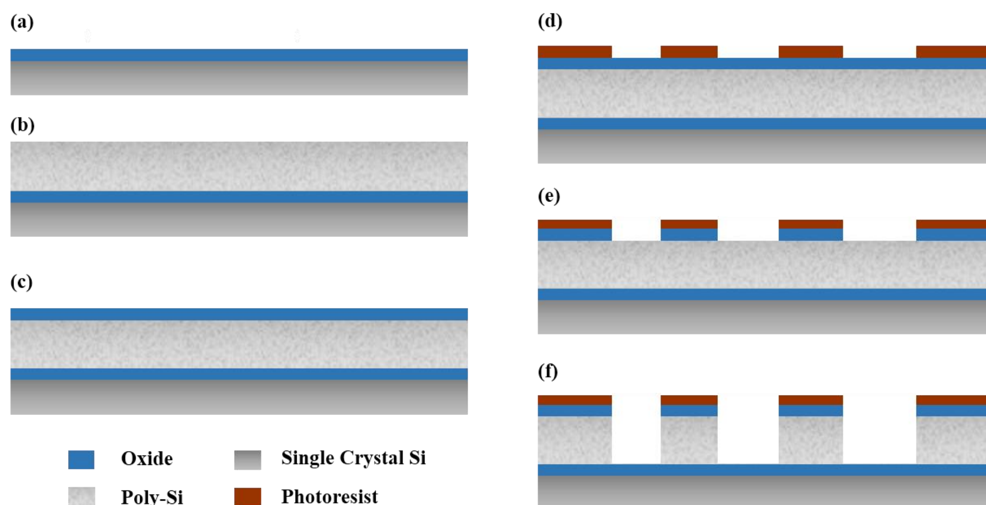


Figure 12: *Polysilicon on oxide wafer fabrication and etch process.*

The SOI etch was performed on polysilicon-on-insulator (pSOI) wafers. The first two passes of the etch were performed to determine that the buried oxide layer was not reached until the 3rd pass, shown in Figure 14a. The etch was performed again incorporating the 3rd pass designed to reduce notching, shown in Figure 14b. It was found that significant notching occurred despite using the recommended settings for SOI etching. Multiple attempts were made at changing tool parameters to curb the notching, but to no avail.

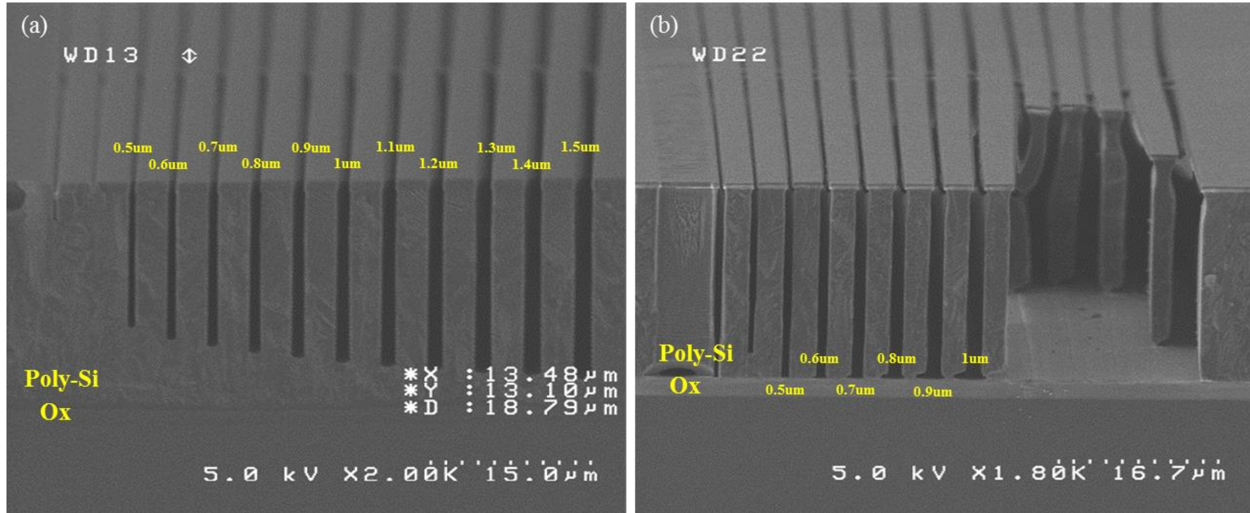


Figure 13: *SOI etch (a) Bulk etch on Polysilicon on Insulator. Loop 1 – 20 cycles; Loop 2 – 34 cycles. (b) Bulk and insulator etch on Polysilicon on Insulator. Loop 1 – 20 cycles; Loop 2 – 34 cycles; Loop 3 – 90 cycles*

The issues observed in PT-DSE are highlighted in Figure 15. Significant notching was found such that the larger trenches were released. Additionally, enhanced blowout and burning of the wafer were seen. The bias pulsing induced by the third waveform in PT-DSE should allow for discharging of the buried oxide layer. However, despite the selected waveform, notching proves to be a significant issue. We suspected malfunctioning of the bias generator to be the cause of these issues. Our test results were reported to SNF staff, and maintenance performed on the tool confirmed the issues with the bias waveform. The pulsing waveform was found to not be within the PlasmaTherm specifications. Further, a 50 Vpp RF noise signal was found in the bias line. SNF is now working on addressing these issues.

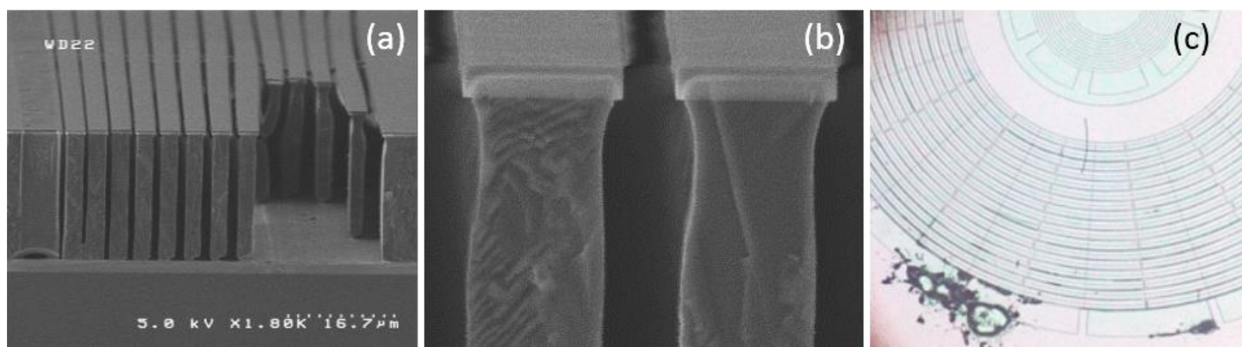


Figure 14: *SOI etching issues in PT-DSE. (a) extreme notching; (b) enhanced blowout; (c) burnt wafer.*

Meanwhile, polysilicon on oxide wafers fabricated as described above were sent out to PlasmaTherm for etching to determine the root cause of the notching issue. SEM images of their etch were performed and very little notching was observed. Despite using similar recipes with the same model tool and test structures, we found drastically different results between the tool at SNF and PlasmaTherm. These results, along with the observed noise and waveform issues, lead us to believe that there exists a tool level issue that prevents SOI etching without notching at the SNF.

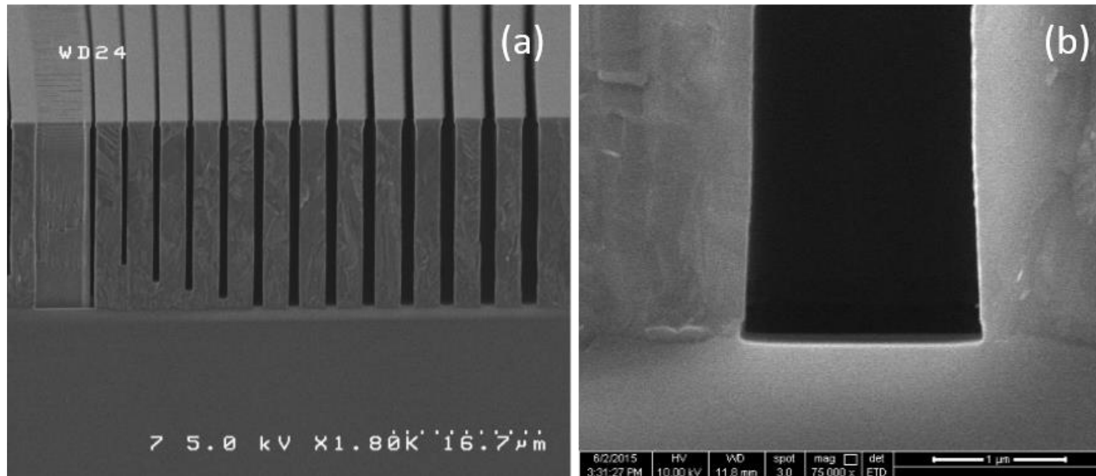


Figure 15: *Polysilicon on oxide wafers etched by PT-DSE at PlasmaTherm. (a) Variable width test structures. (b) Bottom of 1.5 µm trench etched to the buried oxide layer.*

Conclusions

We have developed recipes for variable, high aspect ratio features for both 20 µm and 40 µm etch depths. These recipes have been optimized to reduce the observed aspect ratio dependence, blowout, scalloping, and tapering. Having performed this optimization we find that our results are comparable to work done by groups at Stanford who currently must outsource their wafers for SOI etching. Notching was investigated in the PT-DSE tool at the SNF. Considerable charging issues were observed which prevented the development of a full SOI recipe. The wafers fabricated for recipe development for this project were sent to PlasmaTherm for etching in-house. SEM images of their etch showed proper etch characteristics from their tool. It was determined that further maintenance needed to be performed on the SNF tool to achieve proper SOI etching.

References

[1] Sunil Srinivasan, et al., "Notch Reduction in Silicon on Insulator (SOI) Structures Using a Time Division Multiplex Etch Process".
[2] Andrew Ceballos, Stephen Hamann, "Smooth sidewall etching in the PT-DSE", EE 412 Final Report, Fall 2014.
[3] M. Wasilik and A.P. Pisano, "Low frequency process for silicon on insulator deep reactive ion etching," Proc. SPIE, 4592, 462-472 (2001).
[4] K. Yonekura, M. Kiritani, S. Sakamori, T. Yokoi, et al, "Effect of charge build-up of underlying layer by high aspect ratio etching," Jpn. J. Appl. Phys., 37, 2314-2320 (1998).