EE412 Final Report
Deep oxide etch in Pt-Ox to replace dicing and polishing process

Alex Piggott
Mentor: Usha Raghuram

June 8, 2015

Contents

1 Introduction **2**
1.1 Rationale 2
1.2 Project Description 2

2 Photoresist mask process **5**
2.1 Design of Experiment (DOE) 5
2.2 DOE results 6
2.2.1 Selectivity 6
2.2.2 Sidewall angle 8
2.3 Optimized etch recipe 11

3 Chrome hard mask process **13**
3.1 HDPCVD oxide 13
3.2 Process outline 14
3.2.1 HDPCVD deposition 14
3.2.2 Spinning and patterning photoresist and liftoff layer 14
3.2.3 IntlVac chrome deposition 15
3.2.4 Metal liftoff 15
3.2.5 Pt-Ox oxide etch 15
3.2.6 Pt-DSE DRIE etch 15
3.3 Results 16

4 Conclusion **18**

Appendix A DOE Results **19**

1 Introduction

1.1 Rationale

Optical interconnects have the potential to revolutionize computing by drastically increasing data transfer rates both between and within processors. Silicon photonics is a key enabling technology for low-cost, high performance optical interconnects, and has rapidly matured in the past decade [1].

To characterize integrated silicon photonics devices, light needs to be coupled into and out of on-chip silicon waveguides. One straightforward method for achieving these is to dice and edge-polish the silicon photonic chip, exposing the waveguide facets for butt-coupling into an optical fiber. Unfortunately, when applied to unprotected silicon photonics chips (i.e. no hard protective layer like silicon dioxide), the dicing and polishing process is not ideal:

1. Many waveguide facets ($\sim 20 - 30\%$) are damaged by the polishing process, leading to inconsistent optical coupling.
2. Dirty process that contaminates the chip with polishing debris, also leading to inconsistent coupling.
3. Long turnaround time on the order of 2 - 4 weeks.

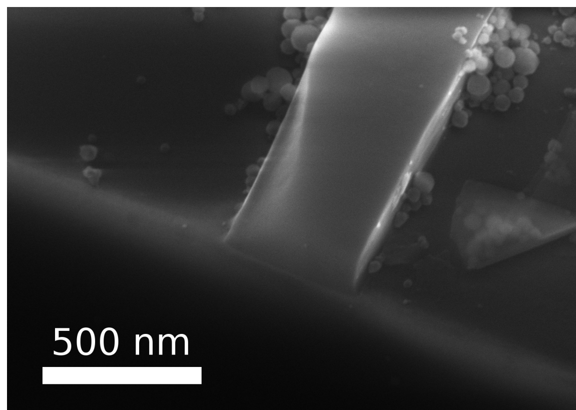

Figure 1: Scanning electron microscopy image of a waveguide facet of a silicon photonic waveguide, produced by dicing and polishing. The waveguide facet is rounded, and a corner of the waveguide facet has been damaged by the polishing process.

Thus, we were interested in developing an equivalent etch-based process to replace the dicing and polishing process.

1.2 Project Description

In this project, we developed a process to etch 100 μm deep, 1 mm wide trenches in silicon-on-insulator (SOI) chips. In the final process, optical waveguides will have already been etched into the silicon device layer by a previous step. The goal of the

etch is to expose the waveguide facets so that light can be coupled in and out of the waveguides via optical fibers.

The SOI substrates considered in this project were SmartCut SOI wafers produced by SOITEC, with a 220 nm device layer and 3000 nm buried oxide (BOX) layer. However, thermal oxide wafers grown in-house were used as surrogate SOI wafers for testing throughout this project.

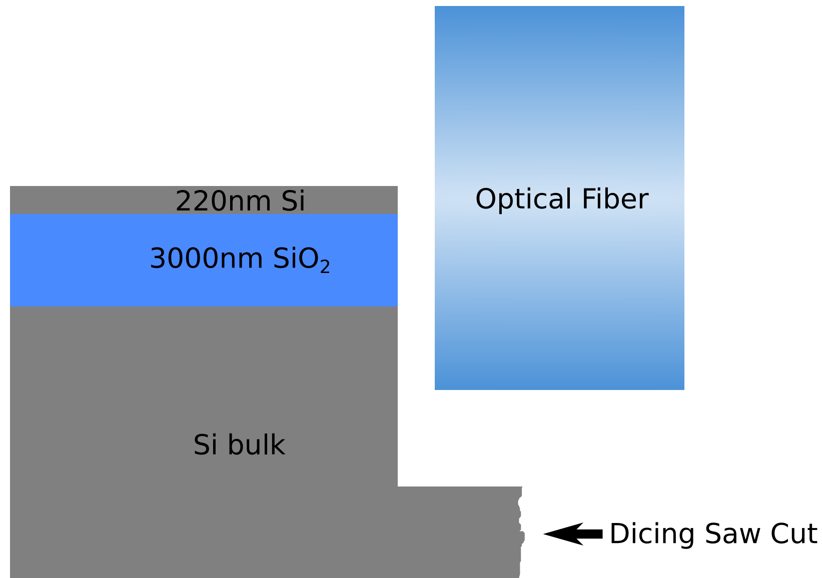

Figure 2: Overview of the completed structure. To edge-couple with fibers, we need to etch through the full wafer stack, which consists of a 0.22 μm silicon device layer, 3 μm buried oxide (BOX) layer, and a silicon handle wafer.

The abridged process is as follows:

1. Pattern mask.
2. **Lampoly / Pt-Ox** etch: 0.22 μm Si device layer
3. **Pt-Ox** etch: 3 μm SiO_2 buried oxide layer
4. **Pt-DSE** etch: 100 μm Si bulk
5. Strip mask.
6. **Dicing saw**: cut through middle of etched trench

The silicon device layer and BOX layer etches must be of optical quality, but the bulk silicon etch can exhibit significant sidewall roughness and scalloping, since its purpose is to provide sufficient physical relief for the optical fiber to couple into the on-chip waveguide.

The buried oxide (BOX) etch was the most challenging aspect of the process, and developing a suitable etch recipe and associated mask was the focus of this project. In particular, the deep oxide etch had the following restrictions:

1. The silicon photonic device layer must be fully protected.
2. The etched sidewalls must be of optical quality.
3. The mask must be selective against both silicon and oxide, and fully removable at the end of the process.

Two different processes were considered: a photoresist-mask process, and a chrome hard-mask process. These processes are described in detail in the following sections.

2 Photoresist mask process

The goal for this portion of the project was to develop a suitable oxide etch recipe for the Pt-Ox etcher, a Plasmatherm Versaline LL-ICP system. No pre-existing process utilizing a photoresist (PR) mask could perform deep oxide etches with vertical ($> 80°$) sidewalls.

The requirements for this etch process are listed in the following table.

Metric	Acceptable Values
Oxide etch rate	> 3500 Å/min
Oxide to PR selectivity	$> 2.5 : 1$
Sidewall angle	$> 80°$
Resist reticulation (burning)	None

Table 1: Photoresist-mask oxide etch requirements.

2.1 Design of Experiment (DOE)

A full factorial experiment was performed on the Pt-Ox using 9 samples. The etch parameters are listed in table 2. Large variations in parameters were chosen in an attempt to span the available parameter space.

Parameter		Value(s)	
Gas Flow	CHF_3	$40, 33, 30$	sccm
	C_4F_8	$10, 17, 20$	sccm
	Ar	5	sccm
Power	ICP	$60, 105, 150$	W
	RF bias	$800, 1100, 1400$	W
Pressure		7	mTorr
Temperature	Electrode	10	°C
	Spool	150	°C
	Lid	150	°C
Backside He	Pressure	4000	mTorr

Table 2: DOE experiment parameters. A 3-variable full factorial experiment was performed, with 8 corners and one center point in the parameter space. Thus, each modified parameter had three etch rates When modifying the hydroflurocarbon flow rates, the total gas flow was kept the same, and only the CHF_3 / C_4F_8 ratio was changed.

The etchant gas ratios, RF bias power, and ICP power were varied in the experiments. The chamber pressure was not varied, as it was believed that it would have a relatively small effect on the process parameters compared with the other variables.

Although a small addition of O_2 to the etch gases was found to improve the sidewall angle for Pt-Ox hard-mask processes, preliminary tests indicated that O_2 tended to make the sidewall angle worse when a photoresist mask was used.

Test wafers were fabricated by growing 1μm thermal oxide wafers in a Thermco thermal oxidation furnace, and then patterning 1.6 μm of SPR3612 resist using an ASML PAS 5500/60 reducing stepper. The test wafers were then cleaved into $\sim 1 \times 1$ cm^2 chips before etching.

The test chips were bonded to silicon dummy wafers using Pentavac 5 diffusion pump oil to provide thermal contact during the etch process. Diffusion pump oil was chosen due to its exceptionally low vapour pressure at elevated temperatures, and ease of removal using solvents or O_2 plasma. After etching, the test chips and dummy wafers were rinsed using acetone and 2-propanol to remove any traces of diffusion pump oil.

The oxide and photoresist (PR) etch rates were characterized using a Nanometrics Nanospec 210XP optical film thickness measurement system. The sidewall angles were measured by taking cross-sectional scanning electron microscopy (SEM) images of multiple (4) etched steps on each chip, and then using a simple MATLAB script to extract the sidewall angles. Before taking SEMs, the samples were cleaned using an O_2 plasma in the Drytek4 Model 100 etcher, and sputter-coated with a thin layer of gold-palladium alloy to reduce charging.

2.2 DOE results

2.2.1 Selectivity

Both the oxide and photoresist etch rates were found to scale almost linearly with the product of the ICP and RF bias power ($P_{RF} \times P_{ICP}$), as shown in figure 3. Remarkably, this trend held even when the etch chemistry was ignored, i.e. changing the $CHF_3 : C_4F_8$ ratio from 3:2 to 4:1 had only a minor effect on the etch rates.

This linear relationship implies that the selectivity between oxide and photoresist stays roughly constant throughout the parameter space we explored. Indeed, we found that the measured selectivity was bounded between ~ 1.7 and ~ 2.4 in our experiments. In figure 4, we have plotted the selectivity as a function of ICP power and RF power. The selectivity goes down slightly as RF bias power is increased, as one might expect from increased ion bombardment. In addition, the selectivity goes up slightly as ICP power is increased, likely due to increased chemical etching from a higher ionization fraction.

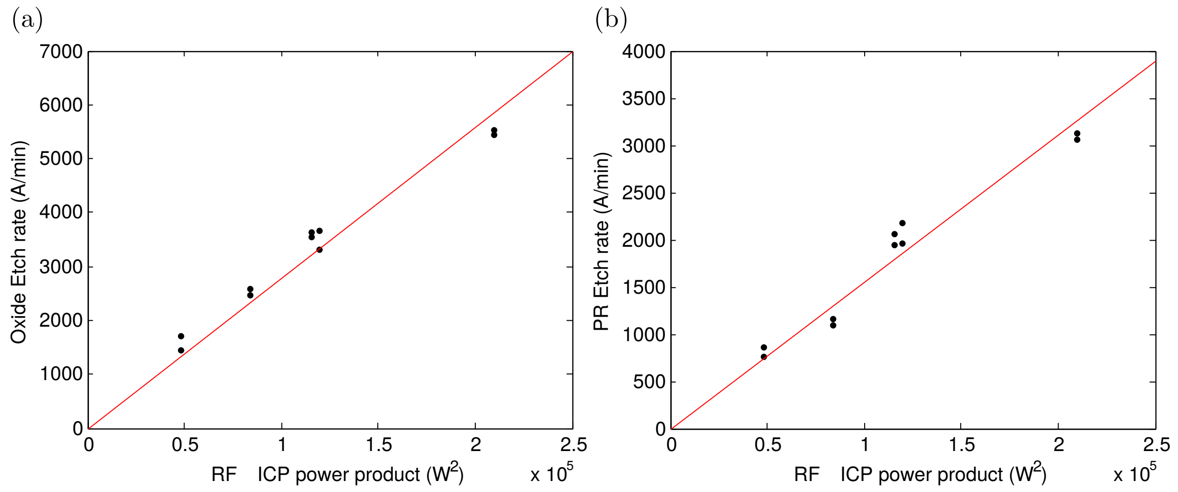

Figure 3: Etch rates as a function of the product of the ICP and RF bias power, for both **(a)** oxide and **(b)** photoresist. The red lines show a linear least-squares fit with the intercept forced to go through the origin.

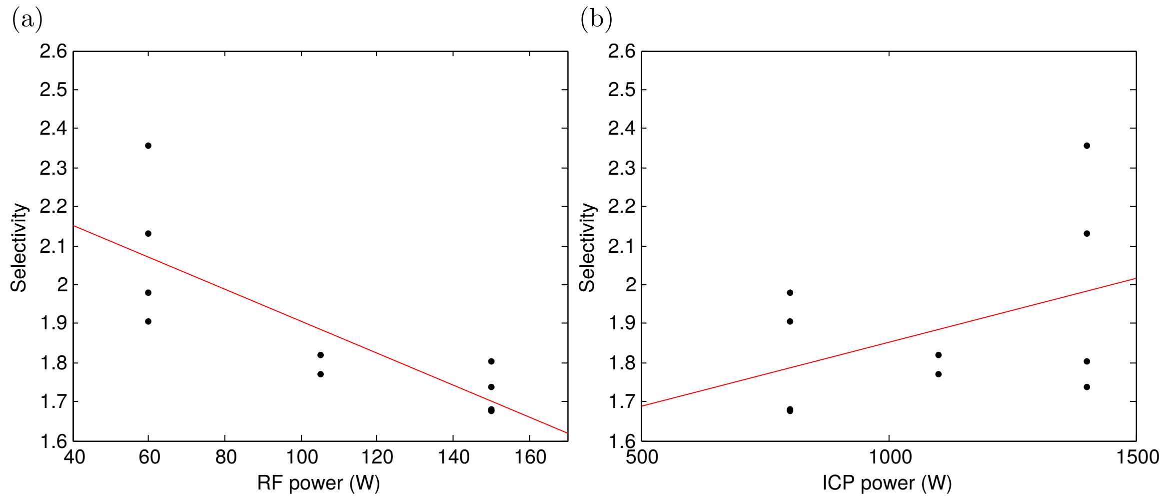

Figure 4: Selectivity versus **(a)** RF power and **(b)** ICP power. The red lines show a linear least-squares fit, but are meant only as a guide to the eye as the trends are unclear.

Unfortunately, we found that the selectively is weakly negatively correlated with sidewall angle. In figure 5, we have plotted the selectivity S against the sidewall angle θ for each condition in our DOE. The correlation coefficient $\rho_{S\theta}$ is -0.1003, which we define as

$$\rho_{S\theta} = \frac{\sum_i \left(S_i - \bar{S}\right)\left(\theta_i - \bar{\theta}\right)}{\sqrt{\sum_i \left(S_i - \bar{S}\right)^2}\sqrt{\sum_i \left(\theta_i - \bar{\theta}\right)^2}} \tag{1}$$

Here, S_i and θ_i are the measured values, and $\bar{S}$ and $\bar{\theta}$ are the mean values.

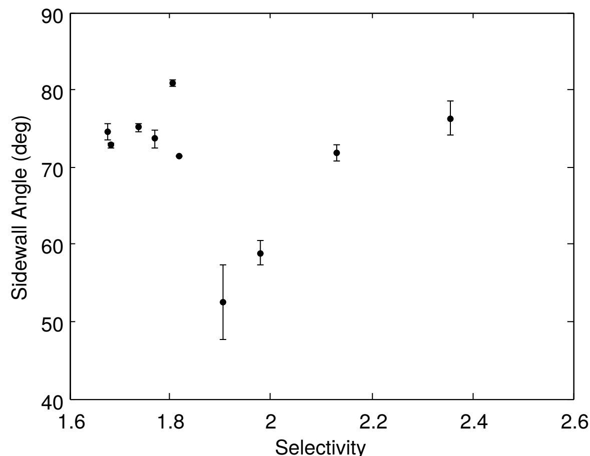

Figure 5: Selectivity versus sidewall angle. The selectivity is weakly negatively correlated with the sidewall angle.

Since we were unable to significantly vary the selectivity of the etch, and the selectivity was weakly negatively correlated with the sidewall angle, we decided to focus on optimizing the sidewall angle. In any case, optimizing the sidewall angle was considered to be more important for replacing the dicing and polishing process.

2.2.2 Sidewall angle

Sidewall profiles for two representative etch processes are shown in figure 6.

Although most etches resulted in straight sidewall profiles, several etch conditions resulted in sidewalls with a double-step shape, as shown in figure 7. The double-step profile appeared in some of the etch conditions with a $CHF_3 : C_4F_8$ ratio of 3:2, but was not present for any other $CHF_3 : C_4F_8$ ratio. It is not clear what causes this double-step shape, although it is likely related to polymer deposition during the etch process, and may be due to a transition between etching regimes halfway through the etch. In these cases, the average sidewall angle was used as the sidewall angle.

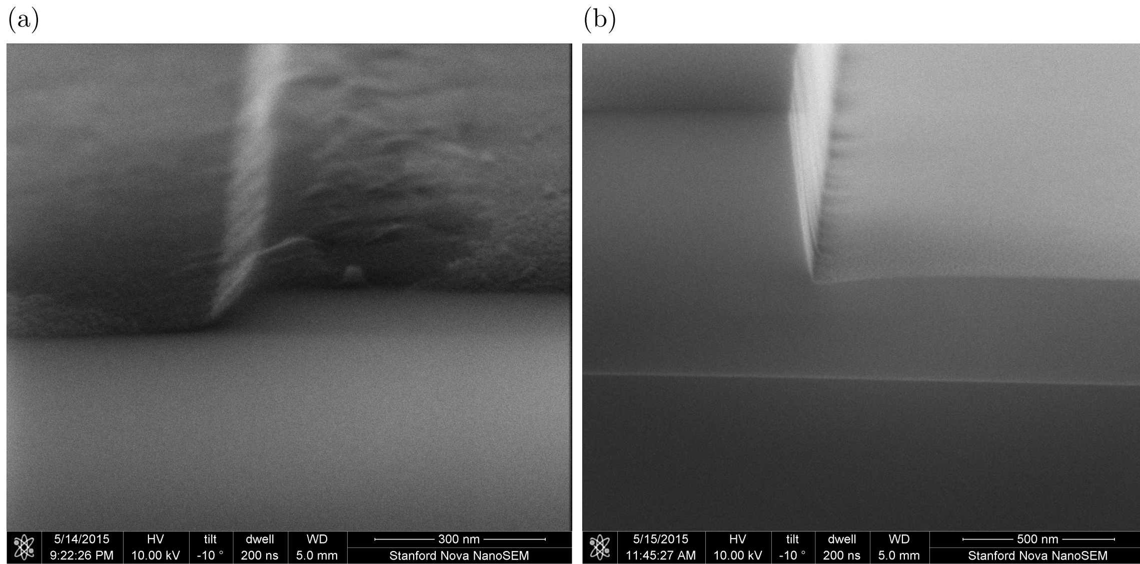

Figure 6: Scanning electron microscopy (SEM) images of sidewall profiles produced by etch conditions **(a)** 3 and **(b)** 8; the etch conditions are described in detail Appendix A. These etch conditions correspond to the least and most sloped sidewall profiles. Some photoresist residue that was not fully removed by the O_2 plasma is visible. In **(a)**, the transition between the thermal oxide and silicon substrate can be seen near the bottom of the image.

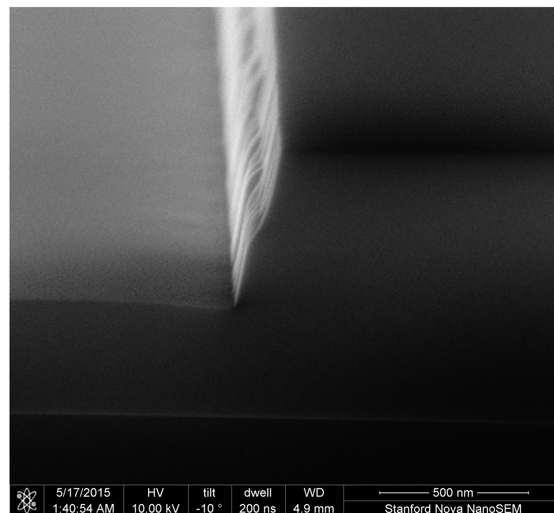

Figure 7: Sidewall profile with a double-step, corresponding to etch condition 9. The etch condition is described in detail in Appendix A.

The sidewall angle as a function of RF bias and ICP power are plotted in figure 8. The sidewall angle is clearly a nonlinear function of RF bias power and ICP power, likely indicating a transition between two etching regimes.

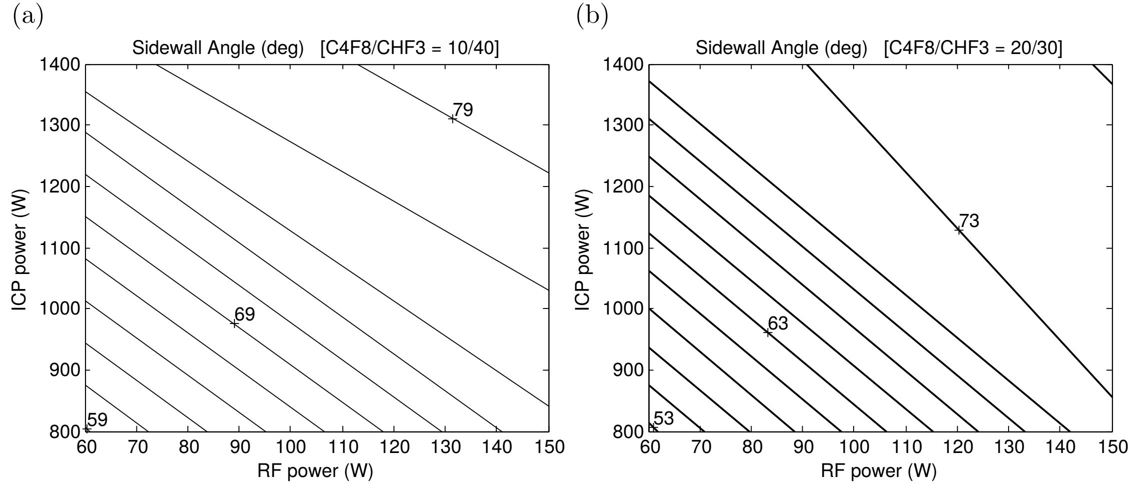

Figure 8: Contour plots of sidewall angle versus RF bias power and ICP power, for CHF_3 / C_4F_8 ratios of **(a)** 4:1 and **(b)** 3:2. Each plot was generated using only 4 points, one at each corner. Each contour corresponds to a step of 2°.

As with the oxide and photoresist etch rates, we found that the sidewall angle was a monotonically increasing function of the product of RF bias and ICP power, albeit rather nonlinear, as shown in figure 9. In addition, there was a small dependence on the CHF_3 / C_4F_8 ratio, with a higher fraction of CHF_3 uniformly corresponding to a steeper sidewall angle.

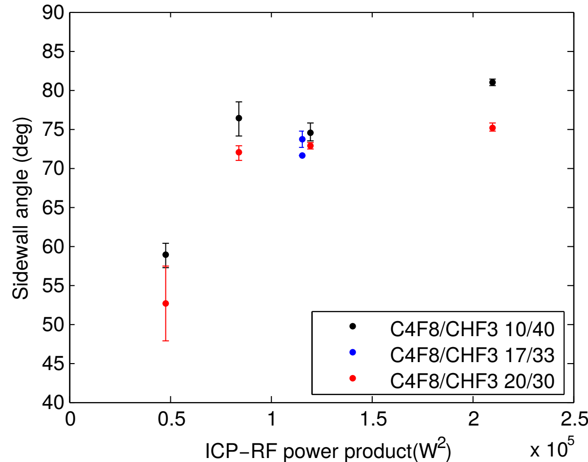

Figure 9: Sidewall angle as a function of the ICP and RF power.

To rigorously determine whether a higher fraction of CHF_3 corresponded to a steeper sidewall angle, we performed the Student's t-test on $\Delta\theta$, the difference in sidewall angle for etch conditions that are identical other than the CHF_3 : C_4F_8

ratio, i.e.

$$\begin{aligned}\Delta\theta\left(P_{RF}, P_{ICP}\right) &= \theta\left(P_{RF}, P_{ICP}, f_{\mathrm{C_4F_8}} = 10\ \mathrm{sccm}, f_{\mathrm{CHF_3}} = 40\ \mathrm{sccm}\right) \\ &\quad - \theta\left(P_{RF}, P_{ICP}, f_{\mathrm{C_4F_8}} = 20\ \mathrm{sccm}, f_{\mathrm{CHF_3}} = 30\ \mathrm{sccm}\right). \end{aligned} \tag{2}$$

Here, P_{RF} and P_{ICP} are respectively the RF bias and ICP power, and $f_{\mathrm{C_4F_8}}$ and $f_{\mathrm{CHF_3}}$ are the C_4F_8 and CHF_3 flow rates. We found that a higher fraction of CHF_3 corresponded to a steeper sidewall angle with significance level $\alpha < 0.05$, and a p-value of 0.00987.

Finally, we tried fitting a linear model to the sidewall angle θ of the form

$$\theta = \alpha_0 + \alpha_{P_{RF}} P_{RF} + \alpha_{P_{ICP}} P_{ICP} + \alpha_r r, \tag{3}$$

where P_{RF} and P_{ICP} are respectively the RF bias and ICP power, and $r = f_{\mathrm{C_4F_8}}/f_{\mathrm{CHF_3}}$ is the ratio between the C_4F_8 and CHF_3 flow rates. The fitted parameters α_x were,

α_0	42.00 °
$\alpha_{P_{RF}}$	0.1216 °/W
$\alpha_{P_{ICP}}$	0.0189 °/W
α_r	-10.20 °

However, the linear fit only reduced the standard deviation of the sidewall angle θ from 8.5° to 3.6°. The predictive power of the linear model is thus dubious at best, considering that we have 4 degrees of freedom in our model but only 9 data points. This was not particularly unexpected since the sidewall angle was clearly a nonlinear function of RF bias and ICP power.

2.3 Optimized etch recipe

The parameters for the final optimized etch recipe are listed in table 3. Here, we chose the etching conditions which lead to the steepest sidewall angle.

The etch could be further optimized by performing a second DOE centered on this etch condition. Based on our results, it appears that a higher ICP power should increase both the sidewall angle and selectivity to photoresist. Further increasing the ratio of CHF_3 to C_4F_8 may also improve the sidewall angle. Finally, other parameters could be explored, such as electrode temperature, pressure, and argon flow rate. Temperature may be a particularly relevant parameter. Certain etch recipes on the Pt-Ox, such as the chrome mask etch process described later in this report, are known to be sensitive to the substrate temperature.

Parameter		Value(s)	
Gas Flow	CHF_3	40	sccm
	C_4F_8	10	sccm
	Ar	5	sccm
Power	ICP	150	W
	RF bias	1400	W
Pressure		7	mTorr
Temperature	Electrode	10	°C
	Spool	150	°C
	Lid	150	°C
Backside He	Pressure	4000	mTorr
Etch Rates	Thermal oxide	5518	Å/min
	SPR3612 resist	3060	Å/min
Selectivity		1.80	
Sidewall Angle		80.88 ± 0.40 °	

Table 3: Optimized etch recipe parameters for the photoresist-mask process.

3 Chrome hard mask process

The chrome (Cr) hard mask process exploits a unique combination of several existing processes to meet the project specifications. The key components of the process are:

1. An excellent chrome hard mask etch recipe developed for the Pt-Ox by fellow labmember Noureddine Tayebi, which results in almost perfectly vertical sidewalls with minimal line edge roughness.

2. The high selectivity between HDPCVD oxide and thermal oxide in 50 : 1 HF, given the proper conditions.

3.1 HDPCVD oxide

Although a chrome mask has sufficient selectivity to perform all three etches that need to be performed (silicon device layer etch, BOX etch, and deep DRIE etch), it cannot properly protect a previously etched silicon device layer. The silicon device layer in our particular SOI substrate is 220 nm thick. Meanwhile, the thickest chrome layer that can be reliably deposited is approximately 100 nm; any thicker and the chrome can easily delaminate due to internal stresses. A chrome mask alone would thus leave sidewalls in the silicon device layer exposed to subsequent etches. A buffer layer which smooths top surface of the chip and protects the silicon device layer is necessary for the chrome mask process.

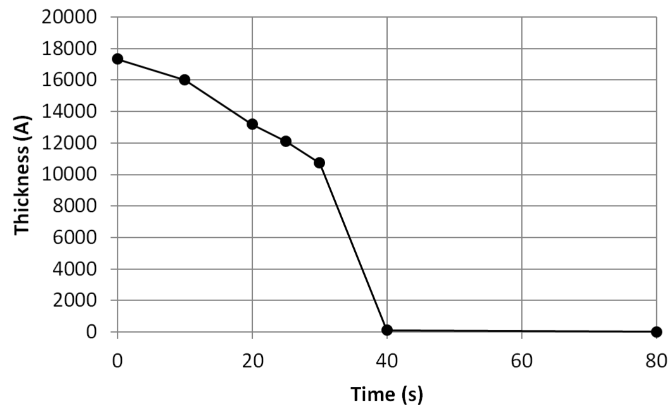

Figure 10: Thickness of HDPCVD oxide remaining after a 50:1 HF wet etch as a function of etch time. The chips were constantly agitated throughout the wet etch to maximize the HDPCVD oxide etch rate. The oxide thickness was measured using a Woollam M2000 spectroscopic ellipsometer. The etch rate clearly increases with time, indicating that the HDPCVD oxide is likely not vertically uniform.

Due to its unique properties, low temperature HDPCVD oxide deposited using the HDPCVD tool is an ideal candidate for this buffer layer. The wet-etch profile of 1.6 μm HDPCVD oxide in 50:1 HF is plotted in figure 10. Meanwhile, the thermal oxide etch rate in 50:1 HF is only ~ 50 Å/min. HDPCVD oxide thus has an effective

selectivity against thermal oxide of $> 200 : 1$, allowing HDPCVD oxide to stripped without significantly affecting the buried oxide layer in an SOI chip.

An important point to note is that constantly agitating the substrate in 50:1 HF increases the etch rate of HDPCVD oxide by a factor of 8 or more, indicating that the etch is probably diffusion limited. Meanwhile, the etch rate of thermal oxide in 50:1 HF is unaffected by agitation, indicating that the etch is likely limited by the surface-reaction rate.

3.2 Process outline

The chrome mask process is as follows.

1. **HDPCVD** deposition: 1.6 μm of HD PECVD oxide
2. Spin and pattern photoresist and liftoff layer (0.2 μm of LOL2000, 1 μm of SPR3612)
3. **IntlVac** deposition: 0.1 μm of chrome
4. Perform metal liftoff.
5. **Pt-Ox** etch: HDPCVD oxide (1.6 μm)
6. **Pt-Ox** etch: silicon device layer (0.22 μm)
7. **Pt-Ox** etch: buried oxide layer (1.0 μm)
8. **Pt-DSE**: DRIE into silicon bulk using the Bosch process (100 μm)
9. Remove chrome using chrome wet etch
10. Strip HDPCVD oxide using 50:1 HF

Test wafers were fabricated by growing 3 μm thermal oxide wafers using a Thermco thermal oxide furnace. The silicon layer was not added to the test wafer stack, as the device layer silicon etch is expected to be the easiest part of the process. The test wafers were cleaved into $\sim 1 \times 1$ cm^2 pieces immediately prior to the etch steps.

As in the photoresist-mask process, the test chips were bonded to dummy wafers using Pentavac 5 diffusion pump oil to provide thermal contact during etching. Silicon dummy wafers were used for the Pt-Ox etches, and thermal oxide dummy wafers were used for the Pt-DSE etch.

3.2.1 HDPCVD deposition

High-density plasma-enhanced chemical vapour deposition (HD PECVD) silicon dioxide was deposited using the standard 90 °C oxide process on the HDPCVD tool, a PlasmaTherm Versaline HDPCVD system.

3.2.2 Spinning and patterning photoresist and liftoff layer

The wafers were spin-coated with 200 nm of Shipley Microposit LOL2000 lift-off layer and 1000 nm of Shipley 3612 photoresist, and exposed using a Karl Suss MA-6 contact aligner system. The standard SNF process was used, as described below.

1. Primed with HDMS (Hexamethyldisilazane) at 150°C using the YES oven.

2. Spin-coated LOL2000 at 3000 rpm for 60 s.
3. Baked for 5 min at 170°C on a hotplate.
4. Spin-coated with 1.0 μm of SPR3612 using the SVG (Silicon Valley Group) coater automated track system.
5. Baked for 60 s on a 190°C hotplate.
6. Exposed using a Karl Suss MA-6 contact aligner system for 1.3 s.
7. Post-exposure bake for 60 s on a 115°C hotplate.
8. Developed for 60 s with MF-26A, followed by a post-develop bake for 60 rm at 110°C, using the SVG develop track system.

3.2.3 IntlVac chrome deposition

1000 Ȧ of chrome was deposited using the IntlVac Nanochrome I Evaporator, an e-beam metal evaporation system.

3.2.4 Metal liftoff

Metal liftoff was performed by soaking the wafers in acetone overnight, followed a 1 hour soak in Microposit 1165 to remove any traces of LOL2000. Finally, the wafers were rinsed using acetone and 2-propanol, and blow-dried using compressed nitrogen.

3.2.5 Pt-Ox oxide etch

The following chrome-mask etch recipe on the Pt-Ox (a Plasmatherm Versaline LL-ICP system), previously developed by Noureddine Tayebi, was used for all oxide etches.

Parameter		**Value(s)**	
Gas Flow	C_4F_8	80	sccm
	Ar	30	sccm
	O_2	10	sccm
Power	ICP	1500	W
	RF bias	80	W
Pressure		7	mTorr
Temperature	Electrode	40	°C
	Spool	150	°C
	Lid	150	°C
Backside He	Pressure	3000	mTorr

3.2.6 Pt-DSE DRIE etch

A 100-cycle Bosch process deep-silicon etch was performed using the standard DSE-FAT recipe on the Pt-DSE tool, a Plasmatherm Versaline LL-DSE system.

3.3 Results

The process was successful on the first run, with no further etch development required. The sidewall profiles after the oxide etch step in the Pt-Ox tool are shown in figure 12. The etch is excellent, with nearly vertical sidewalls and low line-edge roughness. The sidewall profiles after the DRIE etch in the Pt-DSE are shown in figure 12, and here the results are also excellent.

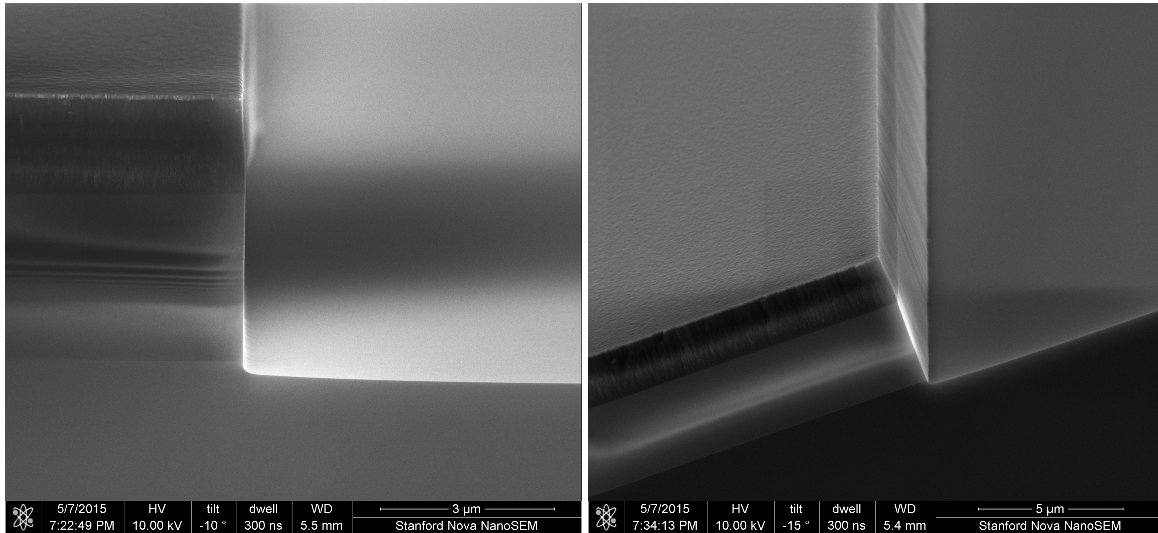

Figure 11: Scanning electron microscopy (SEM) images of the cross-sectional sidewall profile for the chrome mask process after the Pt-Ox oxide etch. Several distinct layers are visible: the $\sim 0.1\ \mu$m chrome mask, the 1.6 μm HDPCVD oxide layer, the $\sim 3\ \mu$m thermal oxide layer, and the silicon handle wafer. The sidewall profile is excellent, with nearly vertical sidewalls and low line-edge roughness.

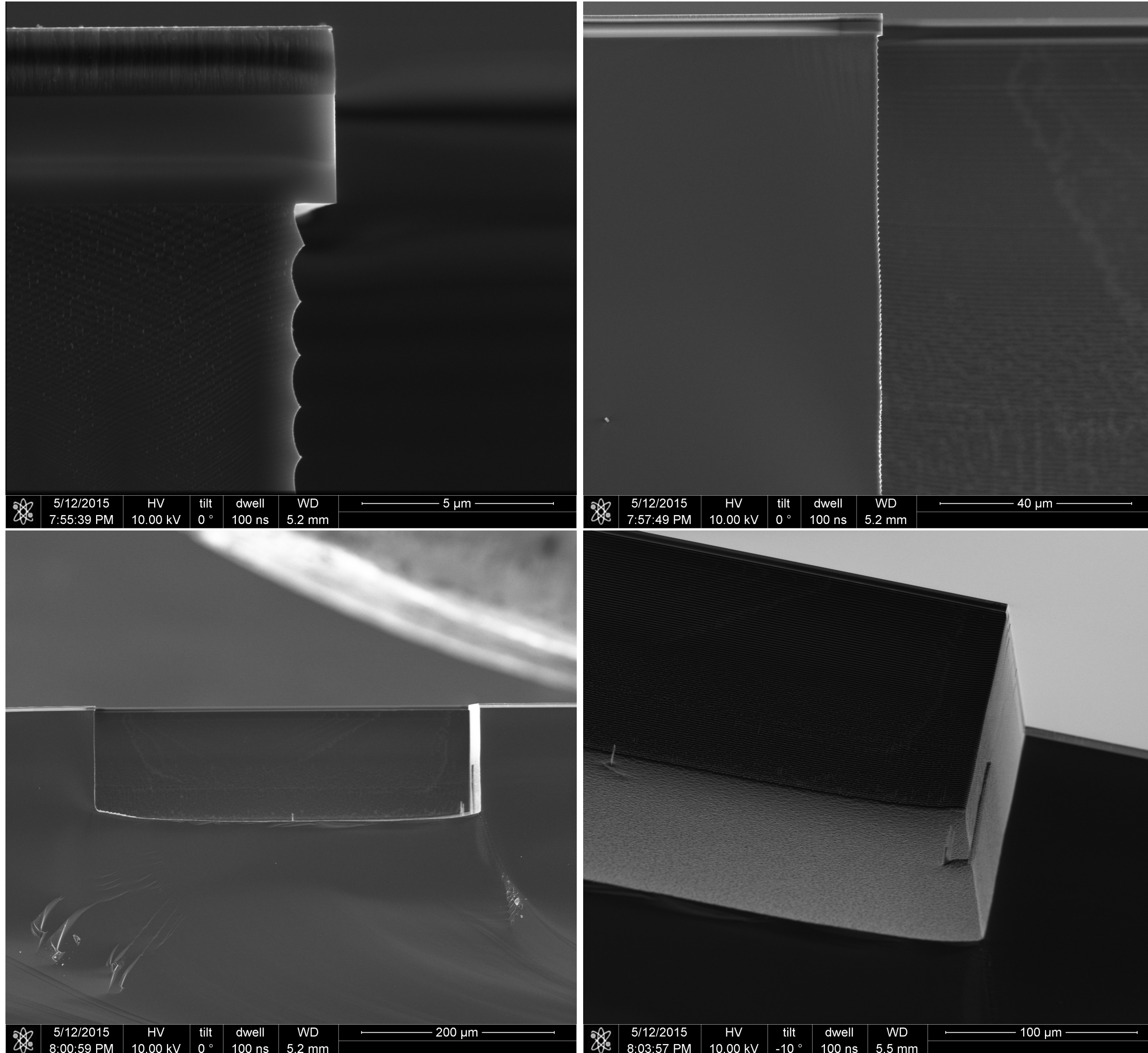

Figure 12: Scanning electron microscopy (SEM) images of the cross-sectional sidewall profile for the chrome mask process after the Pt-DSE DRIE etch, at various magnifications and angles. The chrome mask and HDPCVD oxide layer have not yet been removed. Although the deep silicon etch exhibits significant sidewall scalloping, the sidewall profile is completely acceptable for providing physical relief for optical fiber coupling.

4 Conclusion

We developed an improved Pt-Ox oxide etch process utilizing a photoresist mask by performing a 9-sample full factorial experiment, where we varied the etch gas ratio, RF bias power, and ICP power. We focused on improving the sidewall profile, as the selectivity changed by less than ±20% over the full parameter space of our experiment. In the optimal process we found, achieved a sidewall angle of $80.88 \pm 0.40\,^{\circ}$, a thermal oxide etch rate of 5518 Å/min, and an oxide to photoresist selectivity of 1.80.

In addition, we explored an alternative chrome hard-mask process. Although significantly more complex, this process immediately yielded excellent results, with nearly vertical sidewalls and low line edge roughness.

References

[1] G. T. Reed, *Silicon Photonics: The State of the Art*. Chichester, West Sussex, U.K.: John Wiley & Sons, 2008.

Appendix A DOE Results

ID	Power (W)		Flow Rates (sccm)		**Etch Rates** (A/s)		**Selectivity**	**Sidewall** (°)
	RF	ICP	C_4F_8	CHF_3	Oxide	PR		
1	105	1100	17	33	59.10	32.47	1.82	71.49 ± 0.00
2	60	800	10	40	28.47	14.40	1.98	58.83 ± 1.55
3	60	800	20	30	24.15	12.73	1.90	52.57 ± 4.81
4	60	1400	10	40	42.93	18.20	2.36	76.29 ± 2.18
5	60	1400	20	30	41.05	19.27	2.13	71.89 ± 1.01
6	150	800	10	40	60.80	36.32	1.67	74.58 ± 1.11
7	150	800	20	30	54.98	32.67	1.68	72.78 ± 0.36
8	150	1400	10	40	91.97	51.00	1.80	80.88 ± 0.40
9	150	1400	20	30	90.50	52.08	1.74	75.13 ± 0.54
10	105	1100	17	33	60.70	34.28	1.77	73.64 ± 1.10

Table 4: Pt-Ox DOE experimental results. The modified process parameters and measured values are listed in this table. The etch time was 100 s for all tests.