EE412 Final Presentation

Deep oxide etch in Pt-Ox to replace dicing & polishing process

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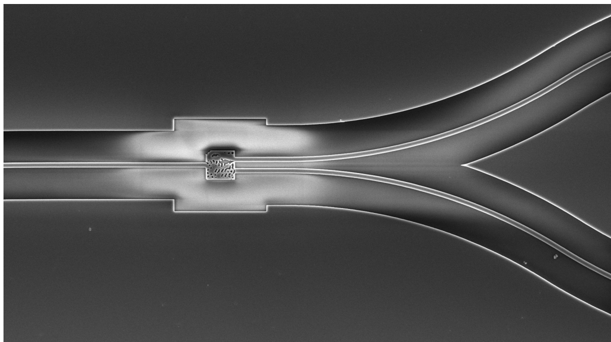
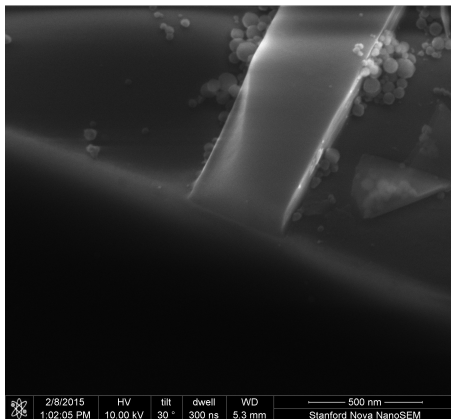


Rationale

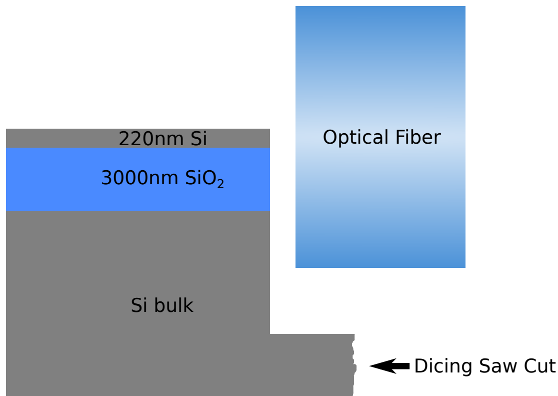
The current dicing and polishing process is not ideal:

- Damage to waveguide facets: unrepeatable measurements
- Dirty process
- Long turnaround time



Basic Requirements

Goal: replace the dicing and polishing process with an etch-based process



Process Overview

The basic process is as follows:

1. Pattern mask
2. **Pt-Ox** etch: 0.22 $\mu\mathrm{m}$ Si device layer
3. **Pt-Ox** etch: 3 $\mu\mathrm{m}$ SiO_2 buried oxide layer
4. **Pt-DSE** etch: 100 $\mu\mathrm{m}$ Si bulk
5. Use dicing saw to cleave trenches
6. Remove mask

Main Challenge: Deep Oxide Etch

The main challenge is etching through the thick $\mathrm{SiO_2}$ layer, with the following restrictions:

- Silicon photonic device layer must be fully protected
- Optical-quality vertical sidewalls
- Mask needs to be selective against both silicon and oxide
- Mask needs to be fully removable at end of process
- If photoresist is used, it needs to survive the etch without reticulation (burning)

Unfortunately, there is no existing process that meets these requirements!

Plan A: Photoresist mask

The proposed process is,

1. Spin and pattern photoresist (4 μm of SPR220-7)
2. Etch silicon device layer (0.22 μm) @ Lampoly
3. Etch buried oxide layer (3 μm) @ Pt-Ox
4. DRIE into silicon bulk (100 μm) @ Pt-DSE
5. Strip mask

The Pt-Ox etch requires significant process development.

Plan A: DOE for Pt-Ox etch

Starting Stack:

1. 1.6 μm SPR3612, exposed at ASML
2. 1.0 μm thermal oxide

Starting Recipe:

- 7 mT, 1400 W ICP, 150 W RF
- C_4F_8 20 sccm, CHF_3 30 sccm, Ar 10 sccm
- 10° C bottom electrode, 150° C spool & lid, 70° C liner

Parameters: RF power, ICP power, C_4F_8/CHF_3 ratio

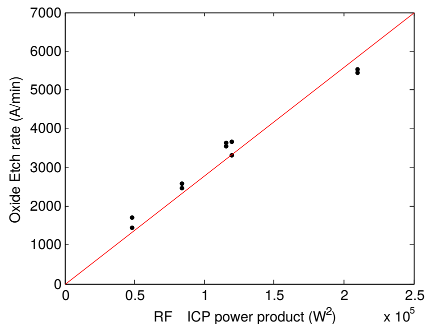
Metrics: Selectivity, (average) sidewall angle

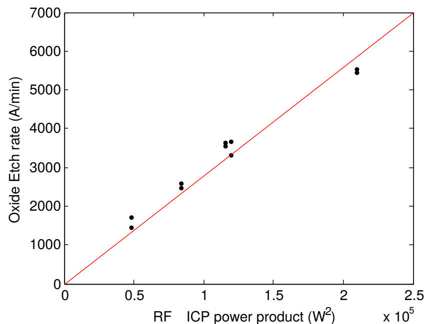
Plan A: DOE results

ID	Power (W)		Flow Rates (sccm)		Etch Rates (A/s)		Selectivity	Sidewall (°)
	RF	ICP	C_4F_8	CHF_3	Oxide	PR		
1	105	1100	17	33	59.10	32.47	1.82	71.49 ± 0.00
2	60	800	10	40	28.47	14.40	1.98	58.83 ± 1.55
3	60	800	20	30	24.15	12.73	1.90	52.57 ± 4.81
4	60	1400	10	40	42.93	18.20	2.36	76.29 ± 2.18
5	60	1400	20	30	41.05	19.27	2.13	71.89 ± 1.01
6	150	800	10	40	60.80	36.32	1.67	74.58 ± 1.11
7	150	800	20	30	54.98	32.67	1.68	72.78 ± 0.36
8	150	1400	10	40	91.97	51.00	1.80	80.88 ± 0.40
9	150	1400	20	30	90.50	52.08	1.74	75.13 ± 0.54
10	105	1100	17	33	60.70	34.28	1.77	73.64 ± 1.10

Plan A: Etch rates

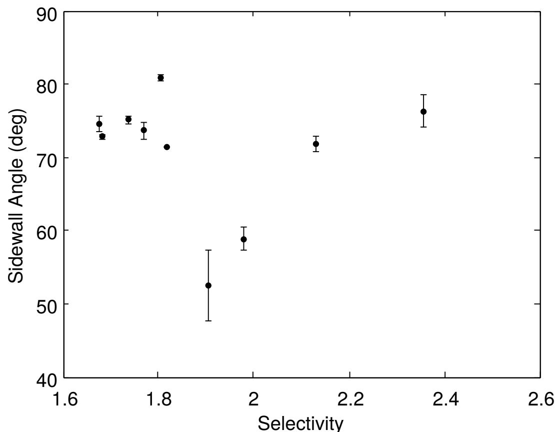
The etch rates are a linear function of the ICP - RF bias power product.





Plan A: Selectivity

The selectivity does not change by more than ±20%, and is weakly negatively correlated with the sidewall angle. We thus focused on optimizing the sidewall angle.



Plan A: Sidewall angles

Here, we show the shallowest and steepest sidewall profiles obtained in the DOE.

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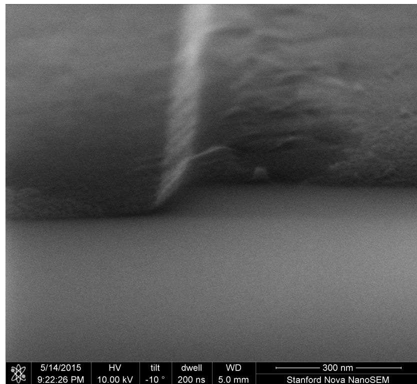

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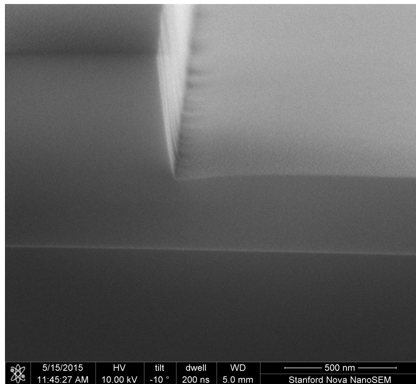
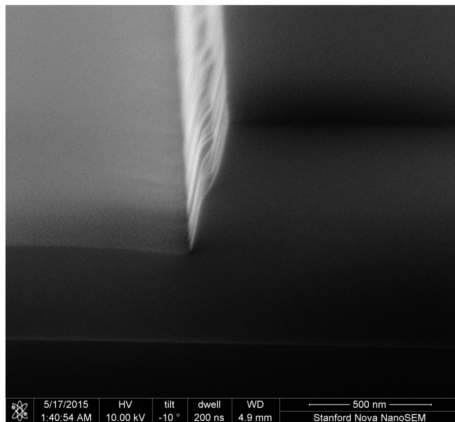


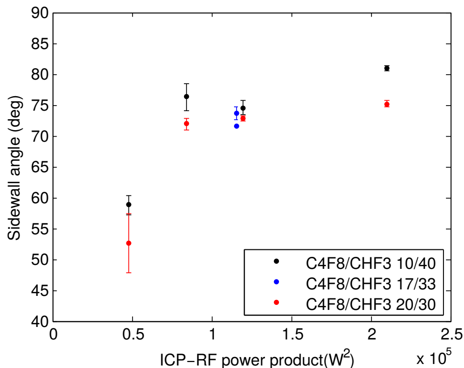
Plan A: Double-step sidewall profile

This curious double-step profile appears in some of the etch conditions. It is not exactly clear what is going on - perhaps a transition between etching regimes partway through the etch?



Plan A: Sidewall angle

The sidewall angle is a monotonically increasing, nonlinear function of the ICP - RF bias power product. Using a $\mathrm{CHF_3} : \mathrm{C_4F_8}$ ratio of 40:10 uniformly resulted in the best sidewall angle.



Plan A: Optimal recipe

The optimal etch recipe (etch condition 8 in the DOE) is,

Parameter		**Value(s)**	
Gas Flow	CHF_3	40	sccm
	C_4F_8	10	sccm
	Ar	5	sccm
Power	ICP	150	W
	RF bias	1400	W
Pressure		7	mTorr
Temperature	Electrode	10	°C
	Spool	150	°C
	Lid	150	°C
Backside He	Pressure	4000	mTorr
Etch Rates	Thermal oxide	5518	Å/min
	SPR3612 resist	3060	Å/min
Selectivity		1.80	
Sidewall Angle		80.88 ± 0.40 °	

Plan B: Chrome and HDPCVD oxide mask

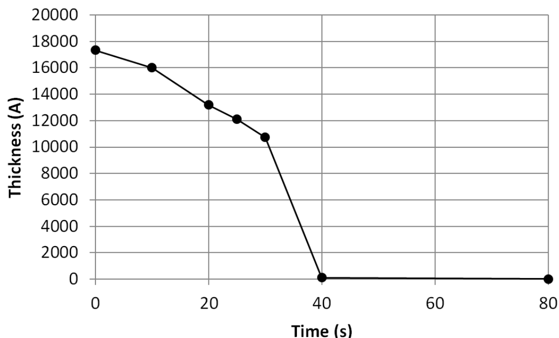
The process exploits the wet etch selectivity between thermal oxide and HDPCVD oxide. The process is,

1. Grow HDPCVD oxide (1.6 μm)
2. Spin and pattern photoresist (1 μm of 3612)
3. Deposit chrome (0.1 μm) @ IntlVac, and then liftoff
4. Etch HDPCVD oxide (1.6 μm) @ Pt-Ox
5. Etch silicon device layer (0.22 μm) @ Pt-Ox
6. Etch buried oxide layer (1.0 μm) @ Pt-Ox
7. Remove chrome using chrome wet etch
8. DRIE into silicon bulk (100 μm) @ Pt-DSE
9. Strip HDPCVD oxide using 50:1 HF

All etches here have already been optimized: an excellent shortcut!

Plan B: HDPCVD etch rate

Measured selectivity of $> 200:1$ against thermal oxide, allowing HDPCVD oxide to be stripped without significantly affecting the BOX layer in SOI.



Important: Must constantly agitate chip to maximize HDPCVD oxide etch rate.

Plan B: Test run design

Starting Stack:

1. 3.0 $\mu\mathrm{m}$ thermal oxide
2. Silicon wafer

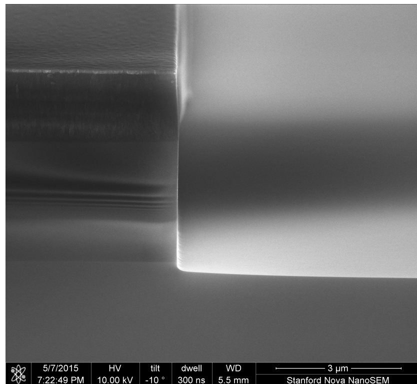
The surrogate test wafer did not include a silicon device layer, as the device layer etch was considered to be the easiest part of the process.

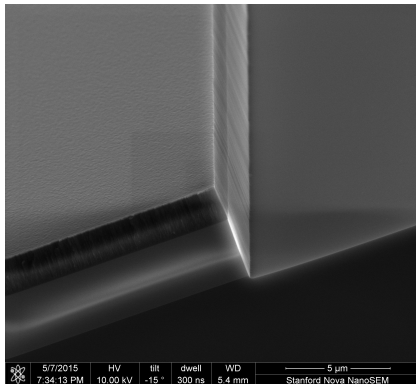
Plan B: Post Pt-Ox etch

Pt-Ox Recipe: provided by Noureddine Tayebi

- 7 mT, 1500 W ICP, 80 W RF
- C_4F_8 80 sccm, Ar 30 sccm, O_2 10 sccm
- 40° C bottom electrode, 150° C spool & lid, 70° C liner

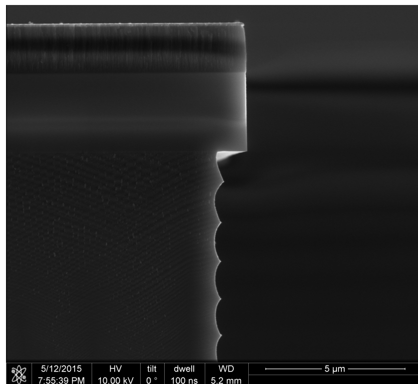
Pt-Ox mask: Cr

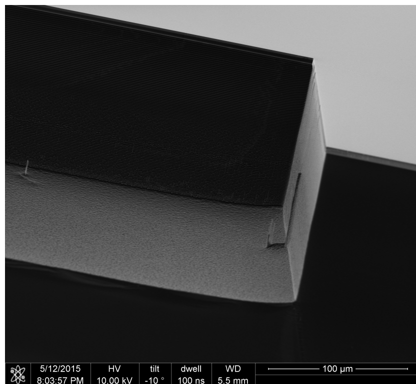




Plan B: Post DSE

DSE Recipe: DSE_FAT @ Pt-DSE
DSE mask: Cr and HDPCVD oxide (not removed in SEM)





- Excellent results (vertical oxide sidewall profile, line-edge roughness, good DSE profile) for fiber-coupling.
- No damage to thermal oxide sidewalls from DSE etch.

Conclusion

Plan A : **photoresist process**

- Performed 9-sample DOE to optimize Pt-Ox etch
- Achieved a sidewall angle of $80.88 \pm 0.40\ ^\circ$, oxide etch rate of 5518 $\dot{\mathrm{A}}/\mathrm{min}$, and oxide to PR selectivity of 1.80.

Plan B : **chrome hard-mask process**

- Measured extremely high selectivity ($> 200 : 1$) of HDPCVD oxide against thermal oxide in 50:1 HF
- Achieved excellent results on first run.