SOP - Released Structures with the PT-DSE

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The goal is to release structures fabricated on silicon from their substrate. In this SOP we present a release process that was tested for structures made of aluminum and lithium niobate that are partially masked by SPR-3612, but the process should be applicable to other materials/photoresist, provided they are not etched by SF_6.

1. Fabricate Structures on Silicon
    1.1. Use your prefered lithography technique and choice of materials to fabricate structures directly on a silicon substrate
2. Write Etch Mask
    2.1. Spin
        2.1.1. Spin photoresist SPR-3612 at 5500rpm for 40s.
        2.1.2. Prebake at 90C for 1 min
    2.2. Expose
        2.2.1. Enable Heidelberg2
        2.2.2. Write CAD patterns with Heidelberg2, optical autofocus, dose = 95mJ/cm^2, defoc = -6
    2.3. Develop
        2.3.1. Enable wbexfab_dev
        2.3.2. Prepare a beaker of MF-26A and a beaker of DI water
        2.3.3. Develop for 20s in MF-26A, rinse for 20s in DI water beaker, rinse additional 20s with the DI sink or gun, blow dry with N2
    2.4. Measure resist thickness
        2.4.1. Use the Nanospec reflectometer to characterize the resist thickness in several locations around one's sample
3. Release Structures
    3.1. Mount sample to 4" carrier wafer
        3.1.1. Place a *small* dab of PMMA on the center of a blank Si wafer
        3.1.2. Place sample on top of PMMA. If the PMMA runs out the sides of the chip you used too much, remove the PMMA in acetone, rinse the wafer and sample with IPA and re-apply the PMMA
        3.1.3. Place the wafer on a 90 C hotplate for 2 minutes to harden the PMMA glue (check that the sample is sufficiently adhered to the wafer by nudging it with tweezers and inverting the wafer)
    3.2. DSE Clean
        3.2.1. Enable the PT-DSE

3.2.2. Insert a dummy wafer (blank 4” silicon wafer) into the PT-DSE, making sure the wafer is pressed against the two screws on the right and the flat is aligned parallel to the mark.
3.2.3. Close the load lock and pump it down
3.2.4. Run DSE Clean for 1800s (30min) on the dummy wafer
3.2.5. When the recipe has finished, open the load lock and re-align the wafer if necessary.

3.3. Condition the chamber
3.3.1. Close the load lock and pump it back down
3.3.2. Run DSE FAT EBTr for 40 loops on the dummy wafer to warm up the chamber and passivate the chamber walls
3.3.3. When the recipe has finished, open the load lock and re-align the wafer if necessary

3.4. Condition the release recipe
3.4.1. Close the load lock and pump it back down
3.4.2. Run the release recipe, “release_iso_target4um” (see recipe details below), on the dummy wafer. This acclimates the tool to the release recipe and avoids encountering unexpected tool errors when processing on actual samples
3.4.3. When recipe has finished, remove the dummy wafer

3.5. Release Structures
3.5.1. Insert 4” carrier wafer with sample mounted, making sure the wafer is aligned correctly.
3.5.2. Close the load lock and pump it down
3.5.3. Run the release recipe “release_iso_target4um” to undercut structures exposed through the etch windows patterned in step 2.
3.5.4. When recipe has finished, remove the carrier wafer

3.6. Measure post-release resist thickness
3.6.1. Use the nanospec reflectometer to measure the thickness of photoresist after the etch. Compare this to the thickness before to obtain the photoresist etch rate.

3.7. Strip photoresist with Matrix
3.7.1. Place carrier wafer with sample into the designated cassette with the flat facing the tool.
3.7.2. Select “Process for Engineers,” select the strip.rcp recipe and verify the time is 350 seconds. We found that 350 seconds stripped at least 500 nm of photoresist
3.7.3. Click “Process for Production.” Click “Auto-run start” and designate the appropriate lot size and slot number.
3.7.4. Start the recipe and remove the carrier wafer when finished

3.8. Unmount sample
3.8.1. Use acetone to dissolve the PMMA glue and free the sample from the carrier wafer.

3.8.2. Rinse the sample and carrier wafer with acetone and IPA, finish by blowing dry with N2

4. Characterize the released structures
   4.1. Take optical microscope pictures
   4.2. Measure the vertical etch rates with a profilometer tool such as the alphastep or dektak
   4.3. Measure the horizontal etch rates under SEM (see nano nugget)

Notes on PT-DSE recipe

The recipe we developed is designed to release structures 4um wide or smaller and comprises the following parameters

Temperature	15 C
Bias Voltage	10 V
ICP Power	1600 W
SF_6:O_2	150:0

If one wishes to release structures of different dimensions we suggest starting from this recipe and adjusting the time. For fine tuning the recipe refer to the results of our DoE found in our final report.

Design choices:

Choosing photoresist: SPR-3612 is the most standard photoresist used and expected etch rates are documented in PT-DSE Operating Instructions on the SNF website. If you're using SPR-3612, you can measure the photoresist etch rate immediately before and after you release your structures using the Nanospec to confirm that the tool is operating correctly.

Profilometry test structures: It is also a good idea to include some test structures that you can use to measure your vertical etch rate when writing the etch mask. These can be simple trenches that you can characterize using the Alphastep after you remove your chip from the PT-DSE and strip the etch mask photoresist.

Anchors and Etch Mask: If you are releasing very wide structures, you may consider making the etch mask smaller than the region between the anchors to avoid the anchors collapsing during the etch.

Editing Recipes in the PT-DSE:

To edit a *sequence*, go to Editor, then Sequence Editor. Note that a sequence calls *steps*. To edit specific parameters (such as etch time or bias voltage etc.) you must edit the parameters in the steps. To do so, click on the step's name in the sequence, then click "Edit this step." This will take you to the Step Editor. Make sure to save the step after you edit it. Go back to the Sequence Editor and once again click the step's name, then click "Replace this step" with your new step. One can also *loop* over several steps in a sequence. This is done in the Loop Editor.

Common PT-DSE Errors:

1. Backside He pressure does not stabilize
    a. The wafer in the PT-DSE is pushed from below by He gas and held snugly in a large ceramic ring with a wafer cutout in the middle. This error message means that the wafer is not well-aligned to the cutout and is usually caused by misalignment by the user when loading the wafer into the loadlock. Always make sure the wafer flat is parallel to the lines on the arm in the loadlock and that the wafer is against the two screws on the arm that are furthest from the Processing Module. Importantly, if the wafer has been removed from the Processing Module between two runs, the user should open the loadlock and realign the wafer. There is also an option to keep the wafer in the Processing Module for multiple runs.
2. Reflected power too high
    a. Although it is not exactly clear what causes this error, a low ICP power (below 1200 W) is a known problem. Further, having too many variables (pressure, gas ratio, temperature, ICP power) changing simultaneously between the so-called Lt (short for "light") step and the main etch (ME) step of the recipe (typically steps 2 and 3, respectively), is also known to cause this problem. One solution is to include a so-called blend step between the Lt and ME steps, where only a few variables are changed between the Lt and blend steps, and the remaining variables are changed between the blend and ME steps.