Plasma activated direct bonding of silicon and lithium niobate thin films

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Introduction

Metasurfaces are two-dimensional arrays of nanoantennas that can control the phase, amplitude, and polarization of light in a subwavelength platform. By carefully designing the geometry of the antenna, these metasurfaces can be used to realize lightweight and mobile optical devices such as beamsteerers and lenses without the need for bulky optical components. Combining a metasurface with an active layer can enable a tunable optical response, further expanding the application space.

Lithium niobate (LNO) is an electro-optically tunable material whose refractive index can be modified with an applied electric field. Its relatively high electro-optic coefficients are particularly useful for realizing tunable photonic devices at low operating voltages. In combination with on-chip photonics, it has been used to demonstrate optical devices that can operate at GHz switching speeds.[1]

The high refractive index of Si allows it to support guided modes. Periodic perturbations to Si nanobars allow free space, normally incident light to excite guided modes in Si metasurfaces.[2] For efficient modulation, it is essential to have the optical mode excited in Si overlap into the LNO layer.[3,4] Thus, the Si and LNO layers need to be in direct contact with each other without an adhesive layer in between. Furthermore, the thermal expansion mismatch between Si and LNO prohibits processing at elevated temperatures.

Thin films of Si and LNO with desired thicknesses for metasurface fabrication are not commercially available bonded together. Surface activated bonding is a technique for bonding dissimilar materials together. By exposing surfaces to a plasma resulting in atomically clean, hydrophilic surfaces with dangling bonds, this technique allows bonding at room temperature. Bonding materials together requires extremely smooth surfaces free of defects, such as particles.

In this report, we describe a process for plasma activated direct bonding of Si and LNO thin films. Following a rigorous cleaning process to remove particles from the surface of the films, the chips are exposed to a O_2 plasma and pressed together. We discuss benefits and disadvantages of using the Flipchip bonder tool for initiating the bond. Finally, we outline a process for removing the backside of a silicon on insulator (SOI) chip to result in a Si thin film sitting on a LNO thin film. A schematic of the main steps in the process flow is shown in Figure 1.

Benefits to the SNF community

Exploring direct bonding of dissimilar materials is beneficial to the SNF community. Typically materials are bonded together using an adhesive layer, which can lead to loss or other detrimental effects in the end device performance. These techniques can be generally extrapolated to fabricating nanophotonic devices that require multiple layers of different materials in thin film form. Additionally, the Flipchip bonder tool typically requires some solder or other adhesive to bond chips. Exploring adhesive-free bonding with the Flipchip tool will expand its capabilities, allowing more users with different bonding needs to use it.

Figure 1. Schematic depicting the bonding and backside removal steps, resulting in a Si thin film sitting on a LNO thin film.

Sample preparation

The presence of particles at a bonding interface can serve as a bane to proper, uniform bonding and can cause a bond to ultimately fail. Therefore, chips were prepared and cleaned thoroughly in order to mitigate particle formation at the interface. 25x25 mm SOI chips, LNO on insulator wafers, and silicon were coated with SPR 3612 photoresist and diced into 5 x 5, 10 x 12 mm, and 10 x10 mm pieces, respectively. Cleaving of the SOI chips and silicon wafers was done using the Flipscribe and hand cleaving tools, and dicing of the LNO on insulator wafers was done using the DISCO wafer saw. The purpose of the photoresist coat was to ensure that any particles formed during the dicing process as well as any particles previously extant on the chip surfaces could be easily removed through the following cleaning procedure. The chips were then cleaned in two steps. First, they were rinsed three solvents: acetone, methanol, and isopropanol, respectively, followed by consecutive 5 minute sonications in acetone, methanol, and isopropanol, and a subsequent blow drying step using N_2. Second, the chips were piranha (9:1 sulfuric acid to hydrogen peroxide) cleaned for 20 minutes at 120 °C, followed by a DI water bath rinse, and a final blow drying step using N_2

Figures and 2a and 2b illustrate a portion of one of our diced SOI chips before and after the two-step cleaning procedure. It is evident that this cleaning process was instrumental in removing both the SPR-3612 photoresist as well as many particles on the chip surface.

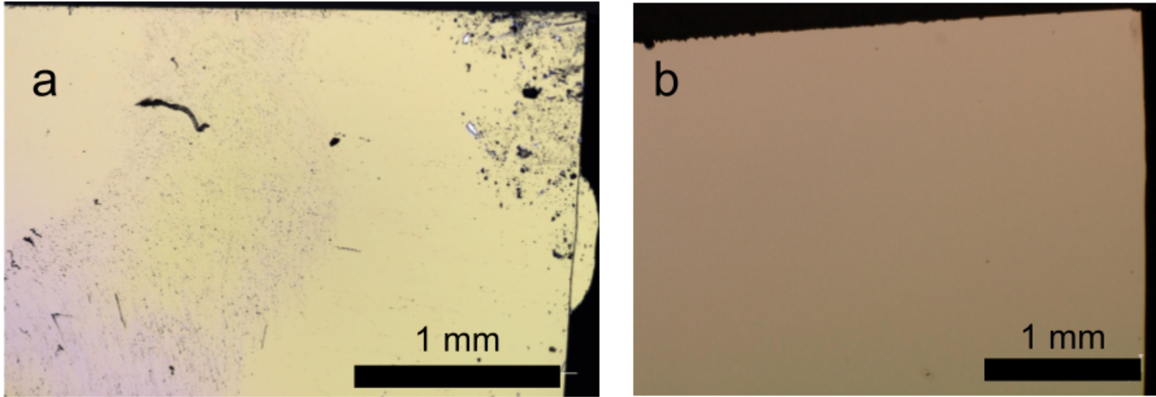

Figure 2. Optical microscope images of a SOI chip (a) after cleaving, coated with photoresist, and before cleaning, and (b) after the cleaning procedure including solvent rinse, sonication, and piranha clean.

Plasma activation and bonding

Plasma activated bonding is a direct bonding technique that can be used to bond dissimilar materials together. The plasma activation process cleans the surfaces of the chips and forms dangling bonds on the surface. The resulting surfaces are very hydrophilic. Following the activation, the chips are dipped in DI water for 30 s. Figure 3 shows a schematic of the water molecules chemisorbed onto the surface of an activated Si chip. The water molecules help initiate the bond through hydrogen bonding between water molecules on opposing chip surfaces. After drying with N_2, the chips can be pressed together to initiate the direct bond. The bonded chips are then annealed in a furnace in our lab (Lindberg Blue). This removes excess moisture from the chips and improves the bond strength. To check if the bond was a success, we picked up the chips with tweezers and held them upside down to see if the top chip would still stick or not.

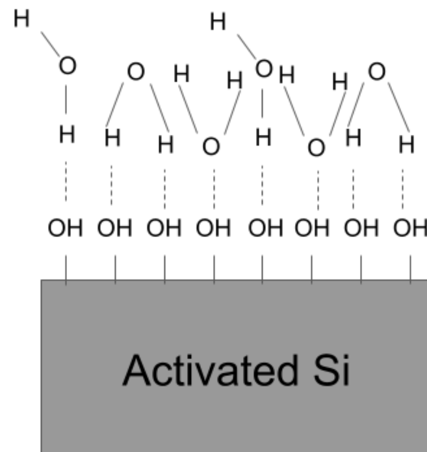

Figure 3. Schematic diagram of a plasma activated Si surface after being dipped in DI water, showing water molecules chemisorbed onto the surface.

Initial trials of bonding Si to Si

To find the optimal parameters for this process and practice running through the procedure, we first studied bonding Si chips together. The chips were cleaved from a larger wafer to 5x5 and 10x10 mm pieces. After the chips have been solvent and piranha cleaned, we exposed the surfaces to a O_2 plasma in the Samco PC300 Plasma Etch tool. This tool is capable of being operated in different modes depending on the shelf on which the samples are placed. The bottom shelf is for plasma etch mode, and the top shelf is for reactive ion etch (RIE) mode. For our process, we chose to use the RIE mode to ensure the plasma activation was sufficiently strong. The recipe parameters were 50 sccm O_2 flow, 250 W RF power, run for 5 minutes. Since we were working with chips, larger wafer pieces were placed around the chips in the chamber to keep them in place.

One of our project goals was to develop a procedure for plasma activated direct bonding using the FInetech Lambda Flipchip Bonder tool. Figure 4 shows a labeled diagram of the tool as well as a schematic demonstrating the bonding operation. This tool has a variable force arm with a die pick to attach a chip to by vacuum. The second chip, also known as the substrate, sits on the heating plate below the arm and is also attached by vacuum. The die pick has a chip contact heating module that allows for heat to be applied to the die chip. The variables we tested were force and temperature. The standby temperature on the Flipchip is 40°C. The ramp rates on both the CCH and heating plate were kept at 4°/sec.

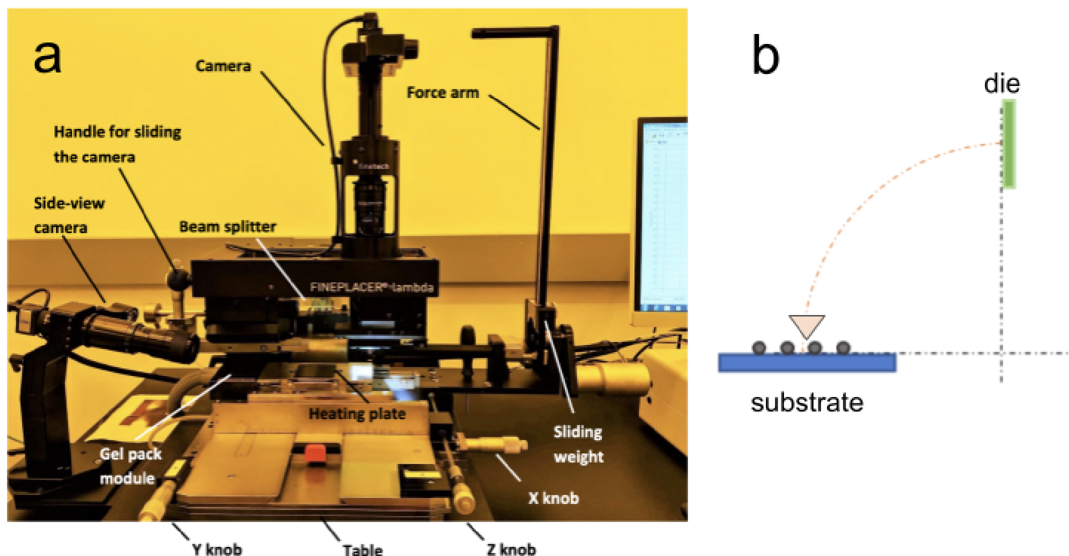

Figure 4. Diagram showing the Flipchip tool and its components labeled and a schematic showing the motion of the die piece to come into contact with the substrate piece to initiate the bond. Figure adapted from the SNF FInetech Lambda Flipchip Bonder Operations Manual.[5]

Initially, we used 15 Pa chamber pressure for the plasma activation and ran the Flipchip tool using various temperatures and forces. After bond initiation, the chips were annealed at 120°C for 1.5 hours. All of these bonds failed after anneal. This led us to consider the chamber pressure as a variable. To focus on the plasma activation, we did not use the Flipchip tool and

initiated the bond with tweezer pressing instead. For pressure values of 60, 90, 120, and 140 Pa, all chips successfully bonded together. Figure 5a shows the chips activated with a 140 Pa plasma pressure after annealing. To test if the bond was a success, we pick the bonded chips up and hold them upside down for a few seconds, shown in Figure 5b, to check if the chips will fall apart. We chose to proceed with a 60 Pa plasma activation as this seemed to be a sufficiently strong plasma activation.

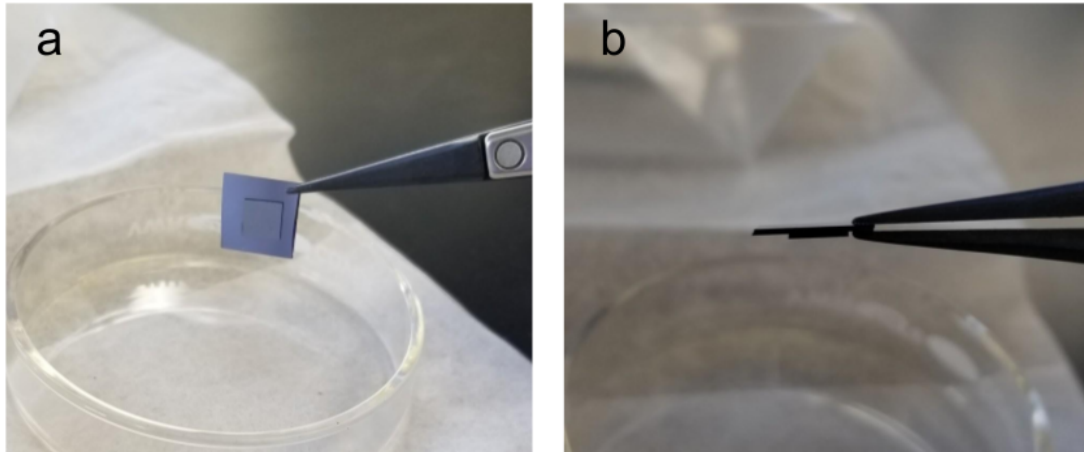

Figure 5. Bonded Si chips using a 140 Pa plasma activation post anneal (a) being held vertically and (b) upside down, showing that the chips are properly bonded together and do not fall apart.

Once the plasma activation pressure value had been chosen, we put together a design of experiment (DOE) to systematically study the Flipchip variables. Table 1 shows the runs for our intended DOE and Table 2 shows the outcomes of our initial trials. The 00 run resulted in a successful bond, while the others failed. To test repeatability of the process, we tried bonding two more sets of chips with the 00 parameters. Additionally, we bonded two sets of chips using 90 N of force to test an upper limit on the force. Our reasoning was that increasing the force would only increase the strength of the bond. These tests resulted in successful bonds, which verified that our process was repeatable.

Table 1. Design of experiment set up to determine the optimal Flipchip parameters

Variable	-	0	+
Force	10 N	50 N	100 N
Temperature	40°C	50°C	95°C

Table 2. Initial DOE runs bonding Si to Si and their bond result.

DOE run	Bond result
--	Fail
00	Success
++	Fail

Through standard amounts of handling, some of the bonded chips would eventually break apart. We began tracking the lifetime of the bond to use as a metric for bond quality. Table 3 shows the bonding parameters and lifetime of the bond, recorded as of May 31, 2021. A '+' symbol indicates that the chips are still bonded together. We found that the chips that were bonded with tweezers more consistently lasted longer than those bonded with the Flipchip. Chips that are properly bonded together should withstand handling in subsequent processing steps without breaking apart. If chips stay bonded together through this handling, the bond is deemed of good quality.

Table 3. Si - Si bonding trials with bond initiation method and length of bond

Bonding parameters	Length of bond (days)
Tweezer bonded	6
Tweezer bonded	37+
Tweezer bonded	37+
Tweezer bonded	37+
Flipchip: 50 N, 50°C	2
Flipchip: 50 N, 50°C	2
Flipchip: 50 N, 50°C	2
Flipchip: 90 N, 50°C	33+
Flipchip: 90 N, 50°C	2
Flipchip: 90 N, 50°C	2
Flipchip: 90 N, 40°C, Tweezer bonded	22+

To determine the necessity of the Flipchip, we tested bonding two sets of chips: one set with no plasma activation, and one set with a 15 Pa activation. Both of these were bonded using tweezers instead of the flipchip. These trials both succeeded and have lasted for longer than 22 days. As such, we concluded that while the Flipchip is useful for when precise alignment and placing is necessary, the force applied with the Flipchip is not enough to have a sufficiently strong bond. It is likely that pressing the chips together with tweezers allows higher forces to be applied over a smaller area, which is essential for a proper bond. The alignment capabilities of the Flipchip are useful when crystallographic axes of your samples must be considered, or one of the chips has a pattern requiring proper alignment. Therefore, we concluded that following up Flipchip bonding with a tweezer press is critical for ensuring a proper bond. We did not continue our DOE for the Flipchip after this point.

Bonding SOI to LNO

After concluding this study with bulk Si chips, we moved to bonding silicon on insulator (SOI) chips to LNO. We used two types of LNO chips: the first trials were conducted with LNO on insulator chips with a 450 nm LNO thin film, buried oxide layer and LNO substrate, and the rest were conducted with LNO on insulator chips with a 100 nm LNO thin film, buried oxide layer and Si substrate. The SOI chips were cleaved to 5x5 mm size pieces, and the LNO was diced to 10x12 mm size pieces. Following the cleaning procedure outlined previously, these chips were plasma activated with a 60 Pa O_2 plasma. After doing a DI water dip for 30 s and blowing dry with N_2, the bond was initiated with the Flipchip tool using 90 N of force at 40°C for 5 minutes. This was followed by pressing the chips together with tweezers to apply extra force. The chips were annealed in the furnace at 95°C for 8 hours. The anneal temperature was decreased from 120°C such that the thermal expansion mismatch between Si and LNO would not cause the chips to debond.

Figure 6a shows the SOI and LNO chips bonded together. Since the LNO substrate is transparent, the bond interface can be directly observed. We notice that there are fringes on the interface, signifying that the bond is not uniform. A closer look shows that there are some particles on the interface, shown in Figure 6b. This is likely contributing to the nonuniformity, as particles would inhibit the two film surfaces from coming into contact with each other. The particles were likely generated during the cleaving process and were not removed properly since photoresist had not been spun onto the SOI piece before cleaving.

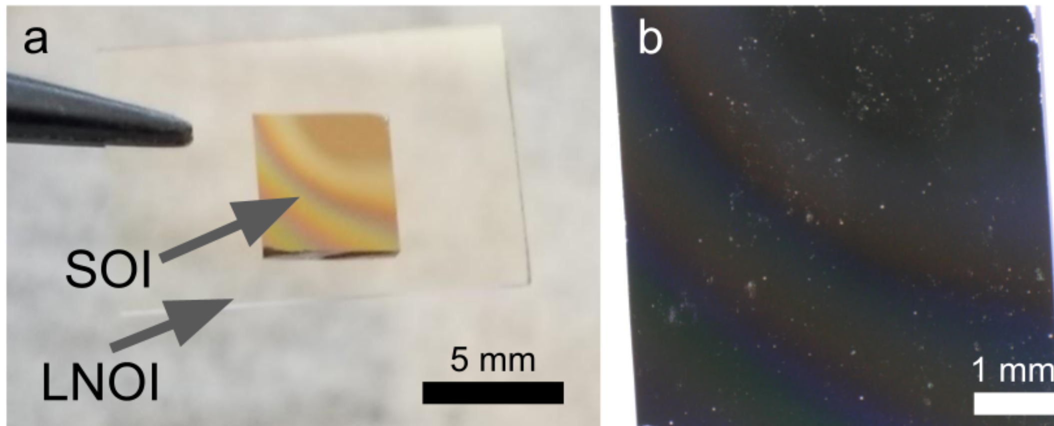

Figure 6. Images of (a) SOI bonded to LNO post anneal and (b) in the optical microscope, with particles visible on the bond interface.

Managing particles throughout the bonding process

To mitigate particle generation from the cleaving process, we started with a new 25x25 mm SOI piece and spun photoresist onto the piece before cleaving. We then continued with our standard cleaning procedure and were able to remove almost all particles from the chip. Since 5x5 mm pieces are quite small, cleaving along crystallographic planes is difficult over such a short distance. This often results in chips with jagged edges. Cleaving larger chips would likely improve the cleave quality and generate fewer particles in the process.

It is important to be mindful of particle generation throughout the bonding process as well. Handling with metal tweezers can scrape the uneven edges of the chips and cause particles to break off and land on the film surface. To avoid this, we used carbon fiber tipped tweezers to reduce scratching of the chips. Before running the plasma activation, the chamber can be wiped down with IPA and a cleanroom wipe. We also visually inspect our chips for particles throughout the process. Occasionally, pieces of dust or other large particles can be seen on the film surface. As such, an optional IPA rinse was included before placing the chips in the chamber. Additionally, the wafer pieces used to frame the chips inside the chamber can be solvent rinsed before placing them in the chamber.

In our final SOI/LNO trials, we started to have bonds more regularly fail. Si and LNO should be harder to bond together than Si and Si since they are dissimilar materials. As such, it is even more essential to manage particles throughout the process. To simplify the process again, we removed the flipchip step from the process and bonded the chips solely with tweezer pressing. We took pictures of the chips after each step in the process to see if particles were being generated from handling along the way. We observed that after the cleaning process, the number of particles on the chip did not significantly increase. However, particles can be generated during the bonding process as well. If there is a particle on the bond interface, it can break up into smaller particles when pressure is applied during the bond initiation. Thus, looking at chips from a failed bond, we can see larger amounts of particles that are likely generated during the bonding steps. Furthermore, the bonding process requires a lot of handling as well during the DI water dip and N_2 dry. This could also lead to particle generation, causing the bond

to fail. Bonding is a tricky and inevitably stochastic process. Great care must be taken to handle chips with caution, manage particles, and keep the surfaces as clean as possible leading up to the bonding.

Backside removal

Because the SOI backside removal process is agnostic to what the SOI is bonded to, we first began the backside removal of an SOI chip bonded to a pure Silicon chip as a test run of our backside removal process.

Backside removal of SOI bonded to Silicon (SOI-Si)

We initially began our backside removal on the Plasma-Therm Deep Silicon Etcher (PT-DSE), under the impression that the SOI backside was solely comprised of a 725 um silicon handle and an underlying 3 um of buried oxide as stated in our SOI chip specifications The PT-DSE is designed to process 4 inch wafers, so in order to etch the silicon handle on our SOI backside, we had to mount our bonded chips onto a 4 inch carrier wafer and then insert the entire carrier wafer into the PT-DSE to etch the backside. To protect the Si carrier wafer from being etched by the PT-DSE, 3.8 um of oxide was deposited onto the Si surface using the PlasmaTherm Shuttlelock PECVD System (ccp-dep) before mounting the SOI-Si chip onto the wafer. The bonded chips were mounted onto the carrier wafer with the SOI backside face up using a small dot of vacuum grease and tapped on using Kapton tape (Figure 7). The Kapton tape was placed around the chip in order to completely cover the exposed sections of the bonded 10 x10 mm silicon substrate, forming a ~ 3 x3 mm window on the SOI backside. The purpose of the Kapton tape was practice for when, in subsequent bonding trials, the SOI would be bonded to the LNO on insulator and we would have to protect the etch chamber from being contaminated by lithium and niobium.

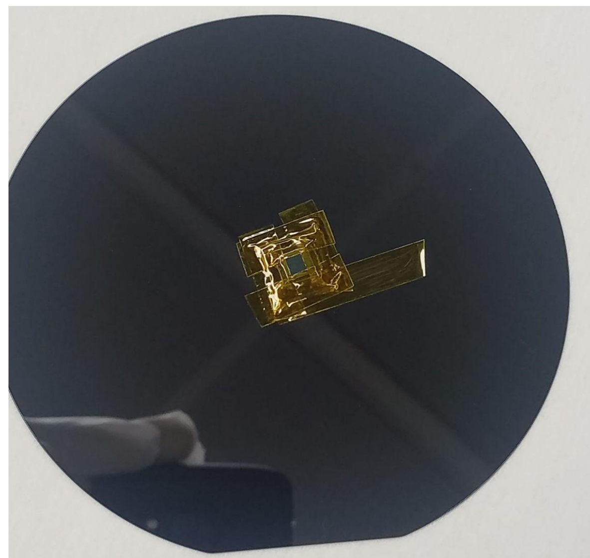

Figure 7. Image of SOI bonded to silicon mounted onto a 4 inch silicon carrier wafer using vacuum grease and Kapton tape

Initial PT-DSE runs proved to be quite perplexing. Even the most aggressive etch recipes would only minimally etch the silicon handle, providing etch rates that were many times slower than expected. Additionally, microscope images of the backside showed a non-uniformly etched surface, suggesting there may be some roughness or some additional layer impeding proper etching. After characterizing a separate, unetched SOI backside with the Nanospec and further discussions with our course mentors, we came to the conclusion that there was ~ 1 um of surface oxide present on the backside likely impeding the silicon handle etch, which was not explicitly stated in the SOI chip specifications. To remove this surface oxide layer off the unetched SOI backside, we used the Oxford Dielectric Etcher (Oxford RIE) with the following standard etch recipe with an expected etch rate of ~250 nm/min:

Table 4: Oxford RIE etch recipe

CHF_3	40 sccm
CF_4	20 sccm
Ar	30 sccm
Power	500 W
Pressure	100 mTorr
He Pressure	10 Torr
Temperature	20 °C

The oxide was etched in 1 minute increments, and after each etch increment, the remaining oxide thickness was measured with the Nanospec, which confirmed the expected etch rate of 250 nm/min as well as visually inspected through film color changes. Figures 3a-3f illustrate the color change in the oxide layer as it is etched away, before etching and after 1,2,3, 4, and 5 minutes of etching, respectively . Within 4 minutes, the previously light blue oxide had been etched away and the underlying surface revealed a grey rough surface, indicative of an unpolished silicon handle.

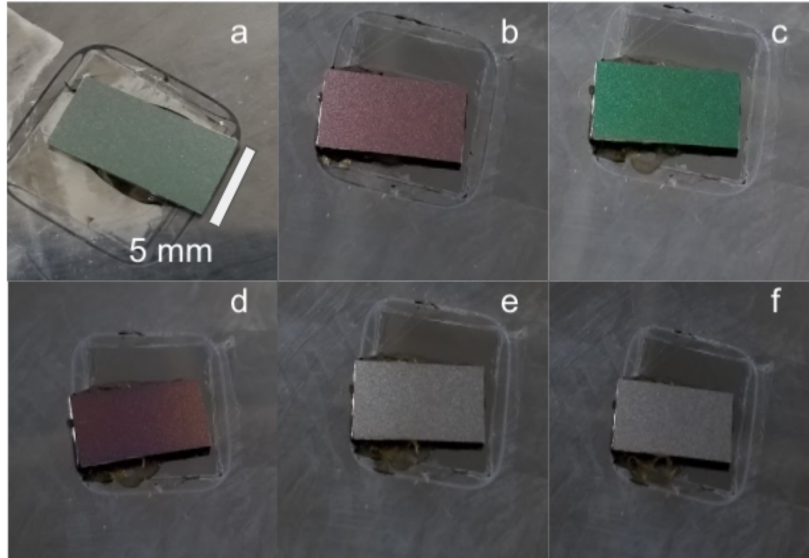

Figure 8. Image of SOI backside (a) before surface oxide etch (b) after 1 minute (c) after 2 minutes (d) after 3 minutes (4) after 4 minutes (5) after 5 minutes of etching with the Oxford RIE

After removing the surface oxide layer, we then used the PT-DSE to complete the Si handle removal on the initial chip we had placed in the etcher. We used the following recipe with an etch rate of ~15 um/min, for 48 additional minutes, after which we were able to completely etch through the silicon handle and reach the buried oxide layer:

Table 5: PT-DSE etch recipe

SF_6	300 sccm
C_4F_8	5 sccm
Ar	30 sccm
ICP Power	3000 W
Bias Voltage	10 V
Pressure	75 mTorr

Figures 9a and 9b are the chip post PT-DSE while on the carrier wafer and under the Keyence Digital microscope, respectively, illustrating the buried oxide layer that is underneath the silicon handle. Figure 9b reveals three interesting features post-PT-DSE. First, there are pink splotches near the corners of the chip. We believe these splotches to be areas of the chip where the PT-DSE had begun etching past the silicon handle into the buried oxide layer. Second, there are roughly micron scale specks that cover the chip, which are likely blisters caused by residual stress in the buried oxide film.[4,6,7] Third, there is wrinkling and some tearing in the underlying silicon film in the bottom portion of the chip.

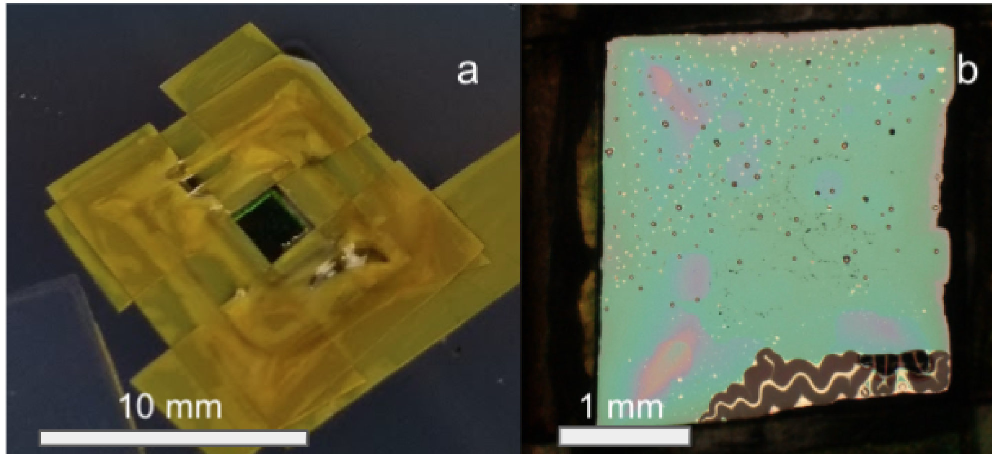

Figure 9. (a) Image of SOI-Si post PT-DSE before removal from carrier wafer (b) bright field microscope image of the SOI-Si chip, illustrating the buried oxide layer

Finally, the SOI-Si chip was removed from the carrier wafer and the underlying 3 um buried oxide layer was wet etched using a 6:1 buffered oxide etch (BOE) solution. Using a plastic pipette, the 6:1 BOE was dropped into the ~ 3x3 mm etch window and etched at 100 nm/ min for 60 minutes. Figures 5a and 5b are the chip after the wet etch and under the microscope, illustrating the silicon film that is underneath the buried oxide layer. It is evident in the bright field microscope image that this silicon film is of poor quality: there are color inhomogeneities throughout the film, intense regions of wrinkling and film tearing at the bottom of the chip, and blisters over the entire area of the chip. To verify that the microscope images were of the silicon film and not of any remaining buried oxide, we then continued to wet etch the chip for 10 minutes. Microscope images taken after this additional wet etch revealed no discernible change in the film, so we remained confident that we had successfully completed the backside removal of the SOI chip. Discussion on how we propose to minimize these blisters and preserve the quality of the silicon film throughout the backside removal process is present in the “Future Work” section.

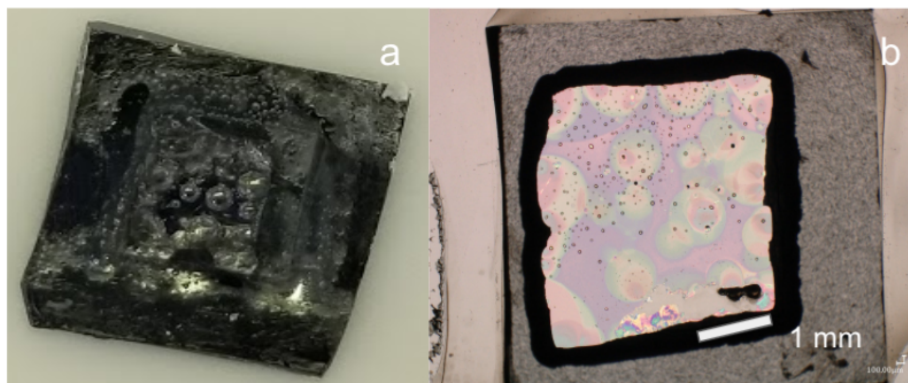

Figure 10. (a) Image of SOI-Si after the 60 minute wet etch (b) bright field microscope image, illustrating the damaged silicon film

Backside removal of SOI bonded to Lithium niobate on insulator (SOI-LNOI)

After our backside removal trial with the SOI bonded to silicon chip, we attempted to remove the backside from an SOI bonded to LNO on an insulator (SOI-LNOI) chip. First, we removed the surface oxide using the Oxford RIE and the etch recipe outlined in the previous subsection. Then, we proceeded to remove the 725 um silicon handle off using the PT-DSE etch recipe stated in the previous subsection. The silicon handle was etched for 46 minutes in 13 minute increments with a 10 minute chamber clean in between each etch increment. Figures 5a-5d illustrate the backside before being etched by the PT-DSE, after 26 minutes of etching, after 46 minutes of etching, and under the microscope post-PT-DSE, respectively.

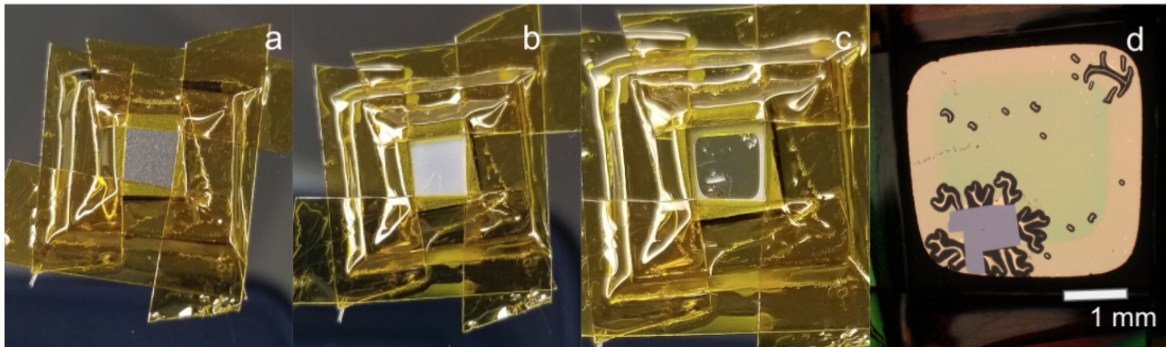

Figure 11. Image of silicon handle (a) before PT-DSE etch (b) after 26 minutes (c) after 44 minutes (d) post-PT-DSE bright field microscope image

The post-PT-DSE bright field microscope image in Figure 11d does not exhibit the same rampant blistering present in our SOI-Si backside removal trial (Figure 9b); however, it does exhibit the same wrinkling and tearing in the silicon film as the SOI-Si backside removal trial. Subsequent removal of the chip from the carrier wafer and cleaning the vacuum grease off of the LNO-insulator backside surface with acetone to begin the wet etch of the buried oxide caused even more wrinkling (Figure 12). This likely occurred due to the rapid cooling of the chips from the acetone clean. Because of this clear decrease in film quality, we did not proceed with the final wet etch step.

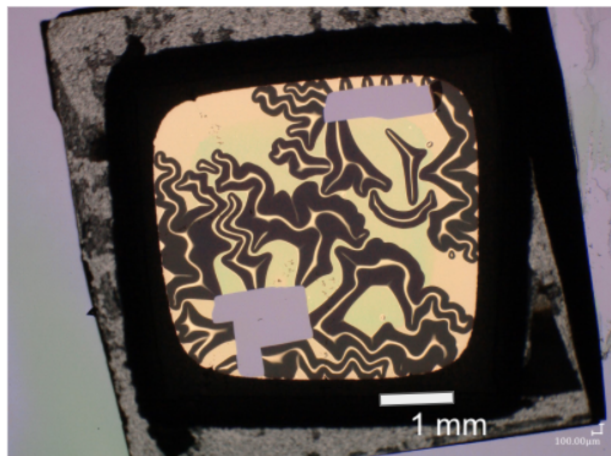

Figure 12. Image of heavily wrinkled film after cleaning of LNOI with acetone before final wet etch step

Future work and conclusion

While we have demonstrated our ability to bond Si to LNO, our yield for this process remains low. Although bonding is a tricky and often stochastic process, further work needs to be done to determine how best to avoid particle generation when handling during the bonding process. We have demonstrated that we are able to clear almost all particles in our cleaning procedure, but the presence of any particles can result in bond failure. Since particles are likely the biggest reason bonds can fail, keeping the surfaces as clean as possible throughout the process is essential.

Working towards fabricating tunable metasurfaces, this process needs to be optimized to preserve the smoothness and uniformity of the Si film. After the backside removal process, we have observed blistering and wrinkling of the thin film, likely due to residual stress in the oxide layer. Attempting this process with a buried oxide layer thinner than 1 um would likely help reduce the amount of blistering. The heat generated during the handle etching step could also contribute to the blistering, and the recipe could be modified to reduce the power near the end of the etch. Furthermore, due to tools being down for extended periods of time, we have not been able to attempt the backside removal process many times. Additional practice will help us determine how best to remove the backside of the SOI chip without damaging the Si film.

Once we are able to successfully remove the backside of the SOI chip and have a pristine Si thin film left sitting on our LNO thin film, the metasurfaces can be patterned and etched with a combination of electron beam lithography and argon ion milling. After successfully demonstrating that Si metasurfaces on LNO can be fabricated, electrical contacts will be patterned onto the chip to enable modulation of our metasurfaces.

In conclusion, we have developed a process to directly bond Si and LNO thin films using a plasma activation technique. For this process to succeed, the surfaces of the films must be kept extremely clean and free of particles. A sufficient amount of force also needs to be applied when initiating the bond, which we found was best delivered with a tweezer pressing step. After bonding Si and LNO, we removed the backside of the SOI chip using a combination of dry and wet etching steps. Further work will be focused on increasing the yield of the bonding procedure and optimizing the backside removal to preserve the quality of the Si film. These procedures will enable the development of tunable metasurfaces and other devices based on dissimilar thin films bonded together.

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Budget

Tool	Cost
samco	$885.85
wbflexcorr-1	$241.67
wbflexcorr-2	$557.5
wbexfab-dev	$160.75
wbflexsolv	$16.67
flipchip	$631.93
PT-DSE	$1342.5
ccp-dep	$100
keyence	$176.74
oxford-rie	$125.83
supplies	$160
Total	$4399.44

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