P-GaN/AlGAN/GaN E-mode HEMT

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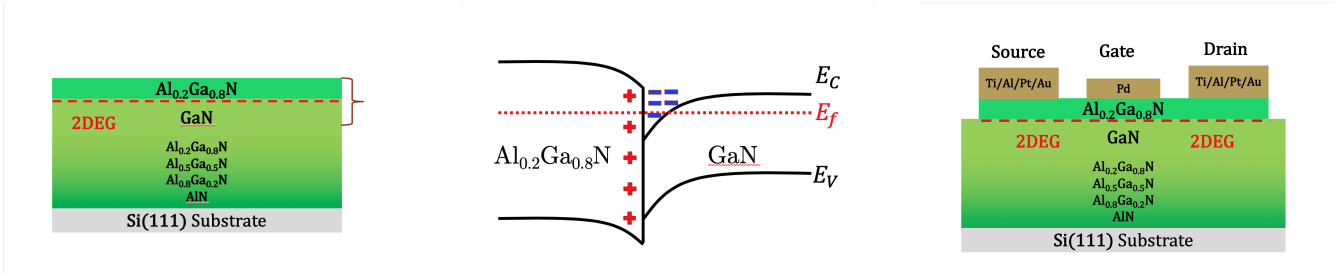
1 Motivation

By **wide-bandgap(WBG) semiconductors** , we refer to materials such as SiC, GaN and diamond whose bandgaps are typically above 3 eV. Conventionally many of them were regarded as insulators rather than semiconductors, but some of their superior properties as summarized in table 1 attracted many people and convinced them to use them as electronic materials. Amongst various interesting wide-bandgap materials, this project is mainly about **GaN(gallium nitride)**. GaN-based heterostructures are frequently employed in high-frequency, high-power, and optoelectronic devices due to their wide bandgap, high breakdown voltage, high electron saturation velocity, and high thermal conductivity and stability[1, 2], just as mentioned above.

Property	Application
Wide Bandgap	Optoelectronics
High Breakdown Field	Power Electronics
High Electron Saturation Velocity	High Frequency Electronics
Thermal Stability	High Temperature Electronics

Table 1: Benefits of Wide-bandgap Materials

However, what makes this particular material especially interesting is the heterostructure of gallium nitride and **aluminum gallium nitride($\mathbf{Al_xGa_{1-x}N}$)** , as in Fig.1a. As $Al_xGa_{1-x}N$ and GaN naturally have different lattice constants, there arises a tensile strain at the interface which causes a **piezoelectric polarization**, which adds to the **spontaneous polarazation** of the material[1]. This polarization causes a net positive charge at the AlGaN/GaN interface, which in turn results in an electron accumulation right underneath it to compensate for this. We refer to this thin quantum well of electrons as in Fig.1a and Fig.1b as **2DEG(2-dimensional electron gas)**.



(a) AlGaN/GaN Structure on Si(111) Wafer with Graded $Al_xGa_{1-x}N$ Buffer

(b) Band Diagram of AlGaN/GaN Heterostructure with Zero Bias

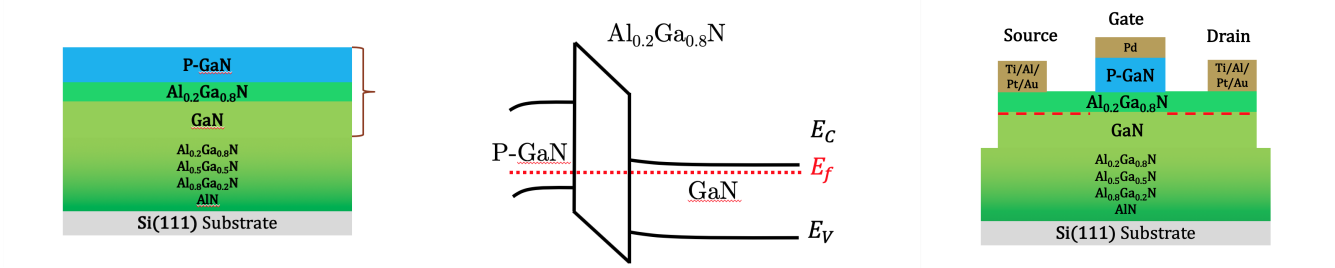
(c) D-mode HEMT using AlGaN/ GaN heterostructure

Figure 1: AlGaN/GaN Heterostructure

Since the high density of AlGaN/GaN 2DEG carriers is not caused by doping, this AlGaN-GaN heterostructure allows us to take advantage of GaN's fast electron mobility as much as possible. Without ionized impurity scattering, we can expect the electron mobility of about $2000\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. Therefore transistors using these structures like Fig.1c

are called **HEMT(high electron mobility transistor)**s. However, these HEMT devices are **Depletion-mode(d-mode) devices** or **normally-on devices** due to the nature of the AlGaN/GaN heterostructure. This makes it significantly hard to design electronic circuits with GaN devices.

Many people have tried to solve this depletion-mode nature of AlGaN/GaN HEMTs and make the devices **normally-off** or **enhancement-mode(e-mode)**. People like Huang et al.[3] and Lanford et al.[4] tried recessed gate structures to suppress 2DEG for zero bias. Other techniques such as fluorine plasma treatment by Cai et al.[5] and ferroelectric materials by Lee at al.[6] were also tried. Another way to achieve an enhancement-mode device would be using materials with proper workfunction to perform **band engineering** and suppress the zero-bias 2DEG. **P-type GaN** doped with Mg acceptors on top of AlGaN/GaN layers can function as such a material[7, 8].



(a) PGaN/ AlGaN/ GaN structure with graded $Al_xGa_{1-x}N$ buffer

(b) Band diagram of PGaN/ AlGaN/ GaN heterostructure with zero bias

(c) E-mode HEMT using PGaN/ AlGaN/ GaN heterostructure

Figure 2: PGaN/AlGaN/GaN heterostructure

Fig.2a shows the PGaN/AlGaN/GaN heterostructure. This p-type doping can be done using Mg dopants during the growth of the layer. As can be seen from the band diagram(Fig.2a), the p-type GaN pulls up the Fermi level and depletes the 2DEG even when there is no gate voltage applied. However, since we have not destroyed the environment in which 2DEG of AlGaN/GaN structure can form, we can retrieve the 2DEG by applying a positive voltage. If we use this heterostructure to build a transistor (Fig.2c), we can have an enhancement-mode transistor utilizing the high-performance 2DEG channel of AlGaN/GaN heterostructure.

If we are successful in this project, the benefits Stanford and SNF can have are as below;

- We have **the first e-mode GaN transistors** at Stanford, which are groundwork for system-level high-power/high-temperature research.
- For the first time we have **control over the threshold voltage of GaN transistors** instead of accepting the value that we measure.
- We will be equipped with **well-controlled etching and growth** for further research with those materials.

Detailed objectives and deliverables are presented in the next section.

2 Objective & Deliverable

This is a continuation of the previous 18-19 Win ENGR241 project of Seungbin Jeong and Anand Lalwani. In perspective of technology development, we can merge two separate recipes SNF had, namely, d-mode HEMT and p-type GaN LED. The ENGR241 project did not end up with a working device due to the failure in characterization of growth and etching of the layers. Therefore, in this project we focus on improved re-characterization followed by the achievement of the original goals of the previous project. The main objectives and corresponding reported materials are summarized below in the Table. 2.

Objective	**Reported materials**
Growth Recipe Characterization	AlGaN growth rate (thickness $t(\tau)$ as a function of time τ) P-GaN growth rate (thickness $t(\tau)$ as a function of time τ)
Etching Recipe Characterization	AlGaN etch rate (depth $d(\tau)$ as a function of time τ) P-GaN etch rate (depth $d(\tau)$ as a function of time τ) I-GaN etch rate (depth $d(\tau)$ as a function of time τ)
PGaN Electrical Characterization	PGaN hole mobility (μ_p) PGaN hole density (p)
Selective Etching Recipe Development	Ox-35 recipe ($d_{AlGaN}(\tau) \ll d_{PGaN}(\tau)$)
Test Device Fabrication	Ohmic contact test result Schottky contact test result Resistor test result Hall measurement result of the suppressed 2DEG
E-mode HEMT Demonstration	g_m-V_{GS} curve I_{DS}-V_{GS}curve I_{DS}-V_{DS}curve (V_{th} and SS extraction)
E-mode HEMT PGaN Variation	g_m-V_{GS} curve (for different t_{PGaN}) I_{DS}-V_{GS}curve (for different t_{PGaN}) I_{DS}-V_{DS}curve (for different t_{PGaN}) $V_{th}(t_{PGaN})$ and $SS(t_{PGaN})$ as functions of t_{PGaN}
E-mode HEMT High-T Characterization	g_m-V_{GS} curve (for different T) I_{DS}-V_{GS}curve (for different T) I_{DS}-V_{DS}curve (for different T) $V_{th}(T)$ and $SS(T)$ as functions of T

Table 2: Objectives and deliverables of the project

The **growth rate characterization** and the **etch rate characterization** are very important starting points, as these were the main reasons for the failure in the previous project. Over-etching or under-etching of the P-GaN layer can either completely isolate or short the contacts and the device would not work as a transistor. Of course, if we can develop a reliable **PGaN-selective etching recipe** the fabrication becomes very easy as we do not need to control the etching duration very carefully. Mg-doped PGaN will also go through **electrical characterization(Hall measurement)** to confirm this is p-type enough.

With well-established recipes, we can fabricate the **test devices**, which are PGaN resistors, I-GaN resistors, AlGaN/GaN 2DEG resistors, PGaN/AlGaN/GaN Hall structures, Schottky diodes and d-mode HEMTs. These devices confirm our etching and growth once more, and test the parts of the e-mode HEMT separately before we fabricate a whole transistor.

After we confirm everything with the test devices we make actual **e-mode HEMT devices** with $t_{PGaN} = 60\,\text{nm}$. After a successful demonstration (a working transistor with a higher V_{th} than that of the d-mode devices from the previous step), we will **vary the PGaN thickness** and will have a control over the threshold voltage of the transistor. We will try 1-2 other thicknesses, but this will be determined after the first set of devices. After all these are done, we will use the same samples for the **high temperature tests**.

With all these done, we expect the following to be deliverable:

- **Ox-35 Nonselective AlGaN/GaN etching recipe and data**
- **Ox-35 Selective (P)GaN etching recipe and data**
- **aix-ccs Mg-doped GaN growth recipe and data**
- **Process-runsheet for e-mode GaN HEMT**
- **Threshold voltage control method of GaN HEMT**
- **High-temperature data of GaN HEMT**

3 Plan

This section presents the expected timeline of the research, along with the tools to be used and a rough estimate of usage and corresponding cost.

3.1 Timeline

We expect this research project to be started by the second week of the April, and to be done by the last week of June. According to the previous experiences from the previous project (ENGR 241), with fully grown layers the post-MOCVD processes take about a week. The timeline presented assume each step is successful within 2 trials.

Time	Research Detail
19.04.08-19.04.14	Growth characterization I (bevelled SEM)
19.04.15-19.04.28	MOCVD growth Growth characterization II Etching characterization I
19.04.29-19.05.05	Etching characterization II Etching optimization
19.05.06-19.05.19	Test structure fabrication Test structure measurement Test structure debugging
19.05.20-19.06.02	HEMT fabrication HEMT measurement HEMT debugging
19.06.03-19.06.16	Varied PGaN HEMT fabrication Varied PGaN HEMT Measurement Modeling
19.06.17-19.06.28	High temperature measurement Documentation

Table 3: Timeline of the project

3.2 Logistics

This subsection talks about the tools or equipment we plan to use. Minimum amounts are estimated assuming (1) we try 2 different PGaN thickness for threshold voltage control modelling, and (2) most of the steps are successful within 2 trials. The maximum amounts are estimated assuming (1) we try 3 different PGaN thicknesses, and (2) most of the stpes are successful within 3-4 trials.

Equipment	**Minimum Expected Cost($)**	**Maximum Expected Cost($)**
aix-ccs	2400	3200
aja-evap	400	800
aw610_r	70	150
DISCO wafersaw	200	300
drytek2	100	150
headway2	150	250
heidelberg	400	700
micromanipulator6000	50	100
Ox-35	800	1600
wbflexcorr	300	600
yes	250	500
zeiss (iLab)	200	400
XE-70 (SNSF)	200	400
Sloped polishing (Glizton shop)	440	440
Total	5960	9590

Table 4: Equipment to be used and corresponding expenses expected

Most of the tools to be used for the project are SNF tools, except for the microscopes (SEM, AFM) and the sloped polishing tool. We use Zeiss SEM of the iLab in Stanford medical school to measure layer thicknesses. Xe-70 AFM from SNSF is needed to measure the etch depth. We are also using sloped polishing tool from Glizton crystal shop located at Spilker builidng. As external mentors advised in the ENGR241, this will magnify the thicknesses measured using SEM.

References

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