P-GaN/AlGAN/GaN E-mode HEMT

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1 Abstract

This community service was a follow-up project for the 18-19 ENGR241 class project **P-GaN/AlGAN/GaN E-mode HEMT**, as the goal of the project was not achieved by the end of the class. The initial objectives of this project consisted of steps: (1) demonstration of E-mode HEMTs using P-GaN layer, (2) investigation of how the layer parameters (doping, thickness, etc.) affect the device performance, and (3) high-temperature characterization of the fabricated devices. Unfortunately, due to the problems including the budget limit,a time-consuming MOCVD equipment maintenance problem and a bad inventory during the COVID-19 shutdown, we only maintained to achieve the first goal. This report will cover how we achieved our first e-mode GaN HEMT at Stanford, process steps, as well as what are needed for improvements.

2 Members of the Project

Seungbin Jeong was the main student of the project. Seungbin Jeong, at the beginning was a student of Stanford X-Lab lead by Prof. Debbie Senesky of AA department. He has currently switched to the Wide-bandgap Group of Prof. Srabanti Chowdhury in EE department. This project was mentored by SNF(Stanford Nanofabrication Facility) staff **Dr. Xiaoqing Xu**.

3 Introduction

3.1 Wide Bandgap Semiconductors

We can start by talking about the **wide-bandgap(WBG)** semiconductor materials for readers not familiar with the concept. By wide-bandgap semiconductors, we refer to materials such as SiC and GaN whose bandgaps are typically above 3 eV. Conventionally many of them were regarded as insulators rather than semiconductors, but some of their superior properties as summarized in table 1 attracted many people and convinced them to use them as electronic materials. Their bandgap values lying in the range of 3 eV to 5 eV allow many optoelectronic devices. As these materials have higher breakdown field values, they can be widely used in the power electronics field. Moreover, their high electron mobility values combined with undoped channel techniques such as modulation doping results in high-performance transistors. Another extremely important property of those materials is that they are very thermally stable compared to conventional semiconductor materials, which makes them a very good choice for harsh environment electronics(e.g. space missions).

Property	**Application**
Wide Bandgap	Optoelectronics
High Breakdown Field	Power Electronics
High Electron Saturation Velocity	High Frequency Electronics
Thermal Stability	High Temperature Electronics

Table 1: Benefits of Wide-bandgap Materials

3.2 Gallium Nitride and 2DEG

Amongst various wide-bandgap materials that show good promises, this project is mainly about **GaN(gallium nitride)**. GaN-based heterostructures are frequently employed in high-frequency, high-power, and optoelectronic devices due to their wide bandgap, high breakdown voltage, high electron saturation velocity, and high thermal conductivity[1], just as mentioned above. Furthermore, GaN devices have demonstrated thermal stability up to 1000 °C in a vacuum, making GaN-based devices of great interest to the high-temperature device community and enabling their use in extreme environment applications where traditional semiconductor materials like Si cannot survive, such as Venus exploration[2]. However, what makes this particular material especially interesting is the heterostructure of gallium nitride and **aluminum gallium nitride($\mathbf{Al_xGa_{1-x}N}$)** , as in Fig.1a. As $Al_xGa_{1-x}N$ and GaN naturally have different lattice constants, there arises a tensile strain at the interface which causes a **piezoelectric polarization**, which adds to the **spontaneous polarazation** of the material[1]. The piezoelectric, spontaneous and total polarization can be modeled as

$$P_{pz}(x) = (-6x + 9x^2)\ \mu\mathrm{C} \cdot \mathrm{cm}^{-2} \tag{1}$$

$$P_{sp}(x) = -10x\ \mu\mathrm{C} \cdot \mathrm{cm}^{-2} \tag{2}$$

$$P_{tot}(x) = P_{pz}(x) + P_{sp}(x) = -16x + 9x^2\ \mu\mathrm{C} \cdot \mathrm{cm}^{-2} \tag{3}$$

This polarization causes a net positive charge at the AlGaN/GaN interface, which in turn results in an electron accumulation right underneath it to compensate for this. We refer to this thin quantum well of electrons as in Fig.1a and Fig.1b as **2DEG(2-dimensional electron gas)**.

3.3 AlGaN/GaN HEMT and Depletion-mode Devices

Since the high density of AlGaN/GaN 2DEG carriers is not caused by doping, this AlGaN-GaN heterostructure allows us to take advantage of GaN's fast electron mobility as much as possible. Without ionized impurity scattering, we can expect the electron mobility of about $2000\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. Therefore transistors using these structures like Fig.2 are called **HEMT(high electron mobility transistor)**s.

However, this HEMT devices are depletion-mode devices due to the nature of the AlGaN/GaN heterostructure. **Depletion-mode devices** or **normally-on devices** are the devices that are turned-on when there is no gate voltage applied. If we refer to the Fig.1b, we can see that when the device is in equilibrium without any external voltage applied, there exists the 2DEG between AlGaN and GaN. Then, if we apply a nonzero drain-source voltage to an AlGaN/GaN HEMT(Fig.2), then the current will flow between two terminals, which means the device is normally-on. Only by applying negative voltage to deplete the channel, the device will turn-off(Fig.1c). Hence the name depletion-mode.

Depletion-mode devices make it significantly hard to design electronic circuits with those devices, as we need to take care of turning off the devices with negative voltage in addition to their normal operation with zero and positive voltages.

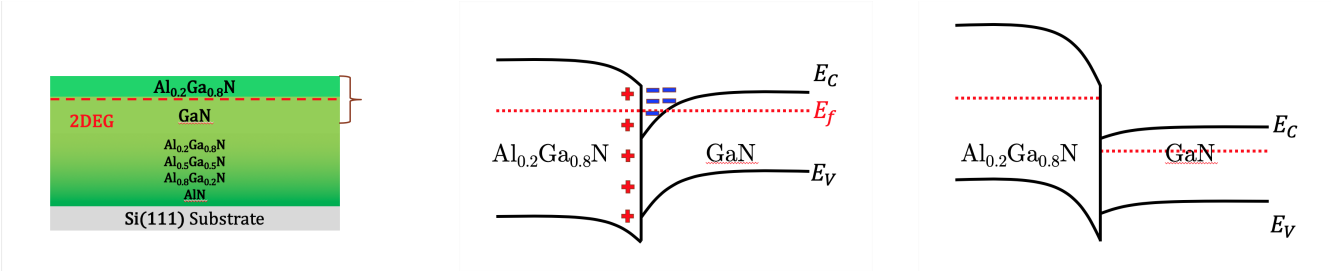
3.4 P-GaN/AlGAN/GaN HEMT and Enhancement-mode Devices

Many people have tried to solve this depletion-mode nature of AlGaN/GaN HEMTs and make the devices **normally-off** or **enhancement-mode(e-mode)**. Enhancement-mode devices are the devices that would not flow electric current when no positive gate voltage is applied. People like Huang et al.[3] and Lanford et al.[4] tried recessed gate structures to suppress 2DEG for zero bias. Other techniques such as fluorine plasma treatment by Cai et al.[5] and ferroelectric materials by Lee at al.[6] were also tried.

Another way to achieve an enhancement-mode device would be using materials with proper workfunction to perform **band engineering** and suppress the zero-bias 2DEG. **P-type GaN** doped with Mg acceptors on top of AlGaN/GaN layers can function as such a material[7, 8].

Fig.3a shows the PGaN/AlGaN/GaN heterostructure. This p-type doping can be done using Mg dopants during the growth of the layer. As can be seen from the band diagram(Fig.3a), the p-type GaN pulls up the Fermi level and depletes the 2DEG even when there is no gate voltage applied. However, since we have not destroyed the environment in which 2DEG of AlGaN/GaN structure can form, we can retrieve the 2DEG by applying positive voltage as in Fig.3c. If we use this heterostructure to build a transistor (Fig.4), we can have an enhancement-mode transistor utilizing the high-performance 2DEG channel of AlGaN/GaN heterostructure.

For us, the primary advantages of using a P-GaN layer are two-fold; first of all, it can be done in the MOCVD machine itself without needs for additional tools. Secondly, current industry standards are using the P-GaN for their own enhancement-mode devices, thus we can keep up with the trend. Currently, SNF has recipes for successful growth of AlGaN/GaN heterojunction layers in the MOCVD process. However, we have lacked the ability to add dopants (in particular, p-type) to this process to grow a layer of P-GaN. Therefore, our MOCVD-based GaN HEMTs that SNF could make were depletion-mode devices. However, now we have a P-GaN recipe for LEDs in SNF. We



(a) AlGaN/GaN Structure on Si(111) Wafer with Graded $Al_xGa_{1-x}N$ Buffer

(b) Band Diagram of AlGaN/GaN Heterostructure with Zero Bias

(c) Band Diagram of AlGaN/GaN Heterostructure with Negative Bias

Figure 1: AlGaN/GaN Heterostructure

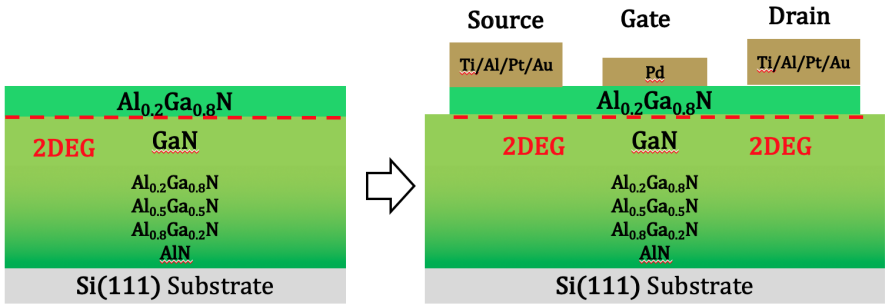
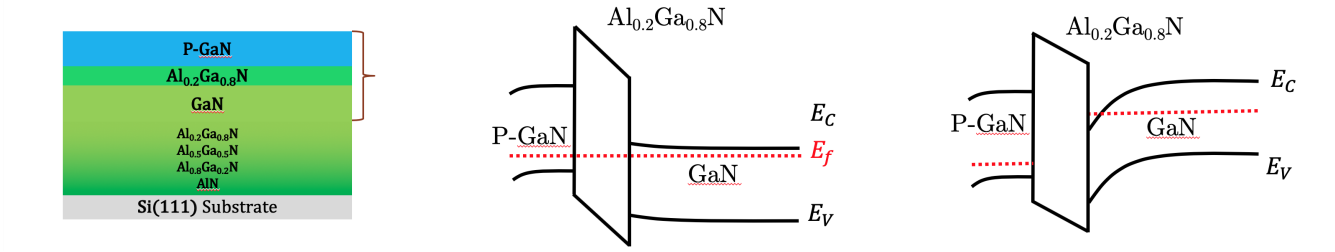


Figure 2: AlGaN/GaN HEMT Structure



(a) PGaN/ AlGaN/ GaN structure with graded $Al_xGa_{1-x}N$ buffer

(b) Band diagram of PGaN/ AlGaN/ GaN heterostructure with zero bias

(c) Band diagram of PGaN/ AlGaN/ GaN heterostructure with positive bias

Figure 3: PGaN/AlGaN/GaN heterostructure

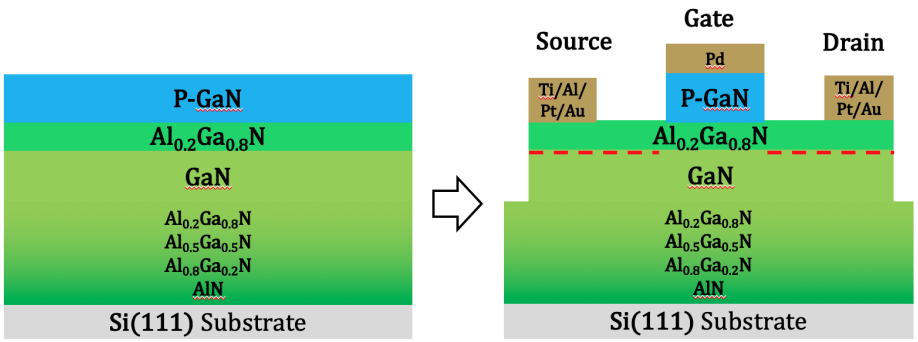


Figure 4: P-GAN/AlGaN/GaN HEMT with Suppressed 2DEG for Zero Bias

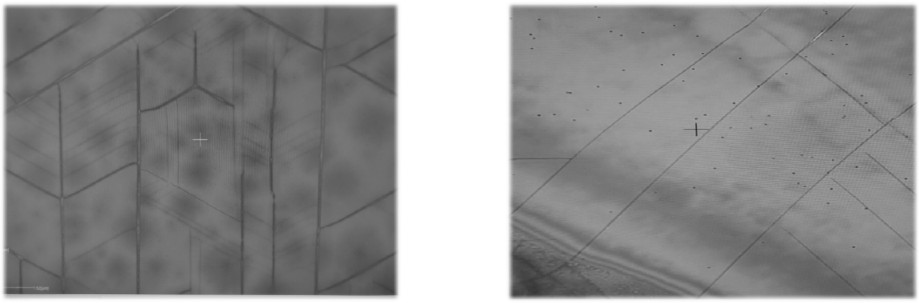


Figure 5: Cracks seen on the surface of gallium nitride samples after the MOCVD growth using Stanford aix-ccs

hope to transfer this P-GaN recipe to the depletion-mode device we have and combine them together to make an enhancement-mode transistor.

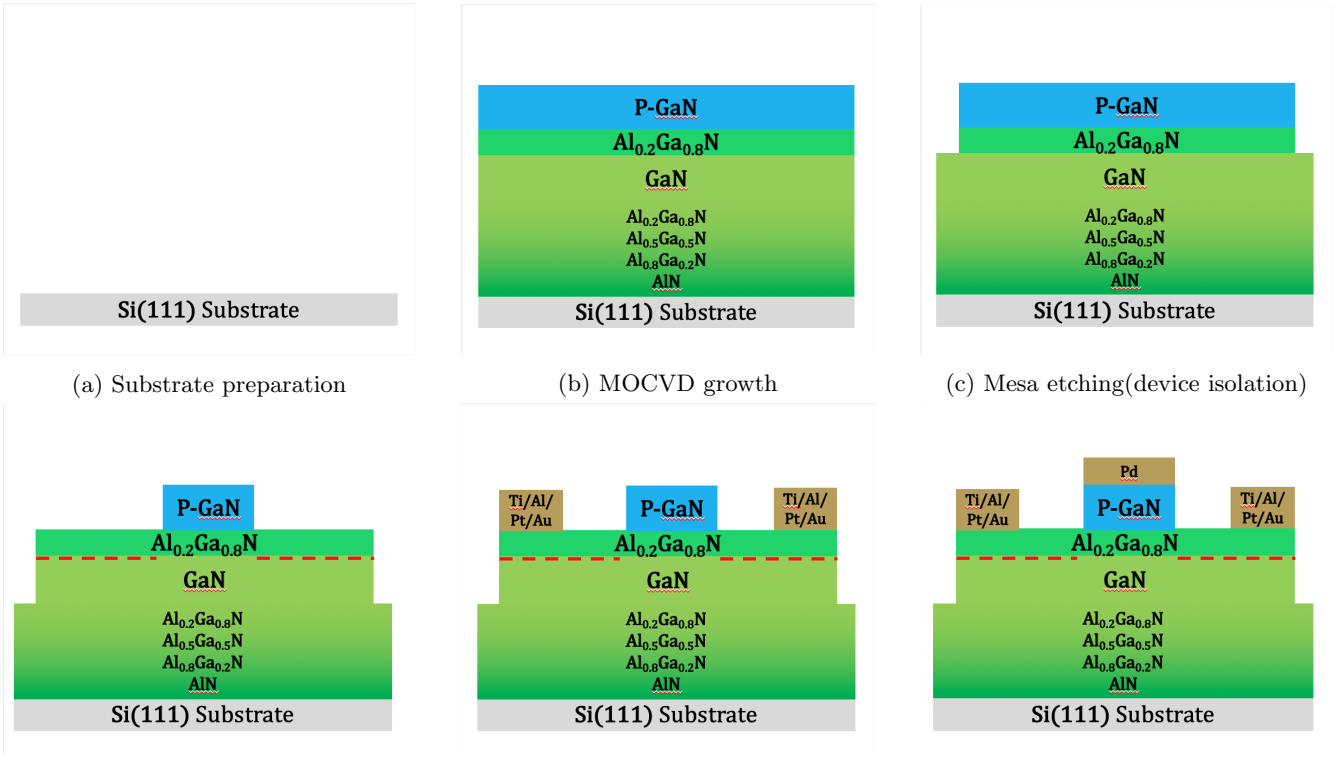
3.5 Objective

The primary objective of the project was the development of a recipe of P-GaN/AlGaN/GaN e-mode HEMTs (using Mg as dopant) in MOCVD, as seen in the Fig. 4. In order to do so, we had to characterize our layers using Hall measurements and cross sectional SEM to verify the electrical properties and growth rate. We wanted to have a working device as a starting point, then investigate optimization parameters including P-GaN doping, P-GaN thickness and AlGaN-thickness. This project also hoped to expand the testing of the devices formed above to see durability and reliability at higher temperatures (up to 700 °C) with the SPI system probe analyser in X-Lab. The main interest of the X-Lab in the GaN devices resided in the harsh environment(high-temperature, high-radiation) applications such as space missions[9]. At the moment the project started, there was little literature available on how P-GaN device performance changes for higher temperatures.

3.6 Limitations

This project encountered several practical limitations. First of all, even with the generous support of SNF, the MOCVD process was very costly. The main parameters we had to modify to achieve our goal were layer parameters such as doping level and layer thickness. Therefore, we had to perform a new growth for each of the sub-experiments, which cost several hundreds of dollars worth of our budget each time. But most importantly, the MOCVD tool aix-ccs had a significant contamination issue for more than 3 months from the April of 2019. Most of our previously developed and characterized recipes for MOCVD did not work, resulting in samples with serious cracks on the surfaces, as seen in Fig. 5 . As our HEMTs were lateral devices with 2DEG channel, those cracked samples could not be used. We managed to modify our previous recipes after a lot of trials and errors. However, by the time that the problem was solved, I (Seungbin Jeong) was inundated by other works related to my main project, and due to the bad inventory work during the COVID19 shutdown lost our samples. Thus, the steps until we could demonstrate our first working device will be the main content of this report.

4 Device Fabrication Method



(a) Substrate preparation (b) MOCVD growth (c) Mesa etching(device isolation)

(d) P-GaN etching(gate definition) (e) Ohmic contact formation(S,D) (f) Schottky contact formation(G)

Figure 6: Device fabrication steps summary

Fig.6 gives us a summary of the whole fabrication process. We prepare a **silicon (111) wafer** as the base substrate. Then we grow the layers using **MOCVD**. After that, we use 2 different masks for etching steps. Fist, we do the device isolation etch (also called **mesa etching**). Second, we do the **P-GaN etching** which leaves p-doped GaN only in the gate area. Next steps are to deposit the source, drain and gate metal contacts. The **Ohmic contacts(S,D)** are formed first, then comes the **Schottky contacts(G)**.

Fig. 7 is an example of our mask design. Just as mentioned above, this mask design consists of 4 layers in total, including the mesa etch protection, P-GaN etch protection, Ohmic metal and Schottky metal. Where the edge of the mesa etching touches the Schottky metal is where we think the majority of the gate leakage comes from. We will illustrate the details in the following subsections.

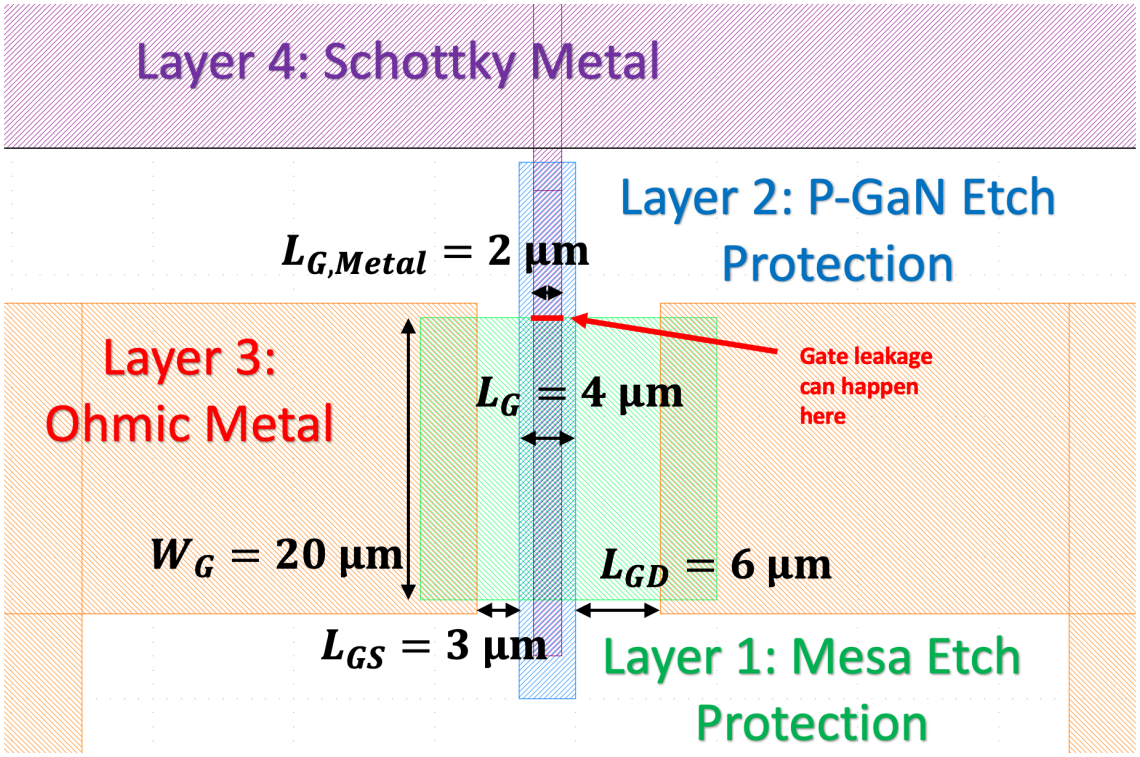
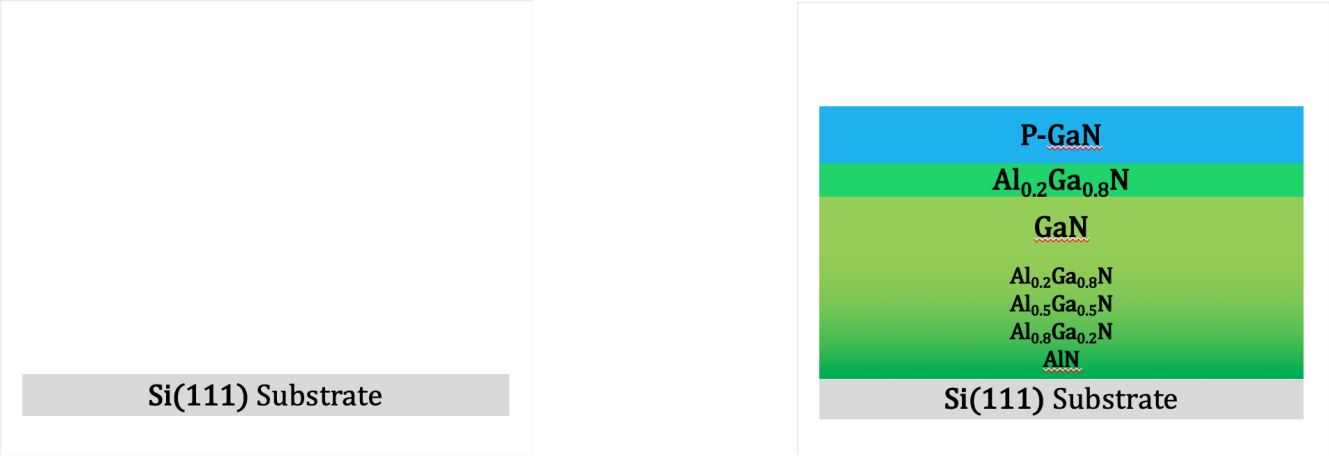


Figure 7: Example mask design for the P-GaN E-mode HEMT. It consists of 4 layers in total: (1) Mesa etch protection (2) PGaN etch protection (3) Ohmic metal for S and D (4) Schottky metal for G. We will discuss it later, but the red line is where the gate leakage is likely to happen.

4.1 MOCVD Growth Of Layers



(a) Sample before MOCVD growth

(b) Sample after MOCVD growth

Figure 8: MOCVD growth of buffer layers, GaN layer, AlGaN layer and PGaN layer

One of the benefits of this PGaN/AlGaN/GaN heterosturcture is that the whole growth can be done at once. However, unlike silicon, we cannot rely on conventional growth processes such as Czochralski pull method, as GaN would decompose into Ga and N if heated.

The way GaN and other complex III-V systems are grown is using a method called **metal organic chemical vapor deposition (MOCVD)**. This method is also known as organometallic vapor-phase epitaxy (OMVPE) or Metalorganic vapor-phase epitaxy (MOVPE). Inside its chamber, the reactant gases which are organometallic(oranic + metal) chemicals, are combined at high temperatures through chemical interaction, resulting in the deposition of materials, mainly III-V compounds. For example, the deposition of a GaN layer can be carried out by the following reaction.

$$\mathrm{Ga(CH_3)_3 + NH_3 \rightarrow 3CH_4 + GaN} \tag{4}$$

Since GaN wafers are not readily available, primary growth of GaN is on Si (111) or SiC and sapphire. The lattice mismatch between Si (111) and GaN is around 17%. To accommodate this lattice mismatch and growth of relatively uniform crystals, a graded buffer layer is grown . This buffer layer consists of $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N}$ where x varies from 0 to 0.2, 0.5, 0.8, as can be seen in Fig.8.On top of these layers, regular AlGaN/GaN layers are grown to form the 2DEG. (The 2DEG AlGaN is $\mathrm{Al}_{0.2}\mathrm{Ga}_{0.8}\mathrm{N}$.) This is basically a regular d-mode HEMT without contacts.

On top of these layers, we grow an Mg-doped GaN layer(P-GaN). One of the benefits of MOCVD is that we can introduce dopants during the growth of the material, which means we can avoid using ion-implantation that can damage the layer. This cap layer is supposed to be only under the gate, hence the rest of this layer is etched out later. Literature states values for P-GaN thickness of 50-80 nm for e-mode devices.

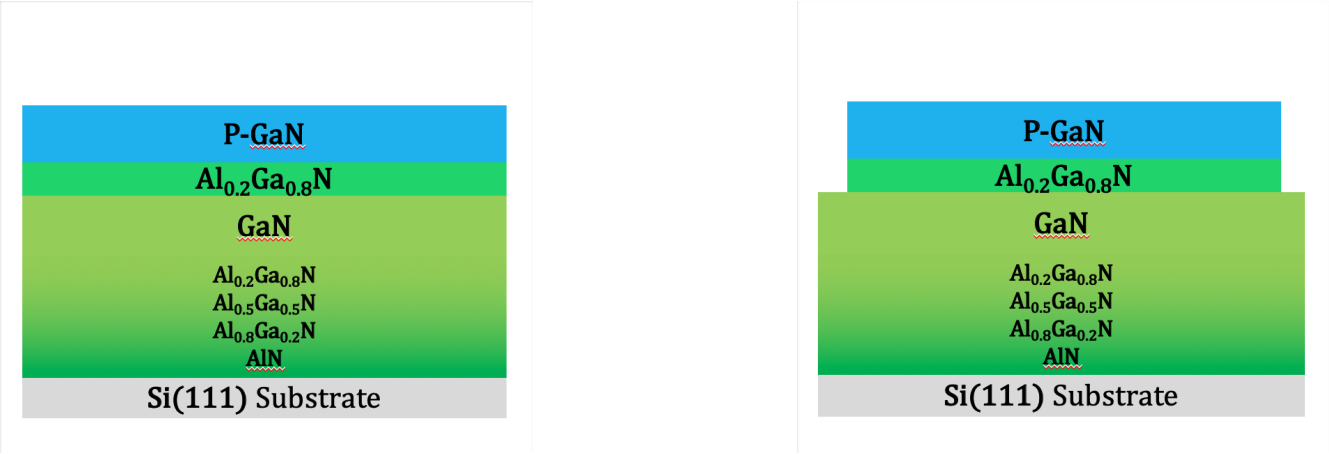
Although MOCVD growth is an incredibly complex procedure and creating new recipes require extensive knowledge of the MOCVD processes, we here list the important aspects of the recipe used by us to grow GaN and PGaN. These recipes built upon existing recipes at SNF and with the help of our mentor, Dr. Xu, we combined them and altered them to fix the previously mentioned contamination and crack problems Units in the table are nm, seconds, mTorr, sccm and °C. For a full recipe, please refer to the recipe **006_pHEMT on Si_heater2**___ in aix-ccs. Its last run ID number was 836 in the log book.

General
TMGa 5°C, 1900mbar (CS16264 was 5°C, 1300 mbar)
TMAl 20°C, 1300mbar
SiH4, 100ppm in H2
Cp2Mg: 15C
Baking
variable Bake_Temp = 1230;
variable Bake_ZnA = 58.8;
variable Bake_ZnB = 62.6;
variable Bake_ZnC = 65.4;
variable Bake_Time = 600;
variable Bake_Time_SiH4 = 600;
variable Bake_Press = 300;
variable Bake_SiH4_Flow = 80;
GaN
variable GaN_Press = 200;
variable GaN_TMGa_Flow = 40.5;
variable GaN_NH3_Flow = 6000;
variable GaN_Time = 1500;#key parameter to solve crack problems
variable Total_Flow_GaN = 12000;
variable GaN_Temp = 1270;
variable GaN_ZnA = 63;
variable GaN_ZnB = 65;
variable GaN_ZnC = 62;
variable GaN_Temp_Final = 1295;
variable GaN_ZnA_Final = 63.5;
variable GaN_ZnB_Final = 65.5;
variable GaN_ZnC_Final = 62;
AlGaN
parameter runtime TwoDEG_Temp = 1280;
parameter runtime TwoDEG_Time = 120;#aim at 12.5 0nm
parameter runtime TwoDEG_Press = 100;
parameter runtime TwoDEG_TMGa_Flow = 7.6;
parameter runtime TwoDEG_TMAl_Flow = 5.5; #25%
parameter runtime TwoDEG_NH3_Flow = 1340/2; #half Gr.
parameter runtime TwoDEG_Cap_Time = 30;
parameter runtime TwoDEG_AlN_Time = 40;
GaN + Mg Doping
variable GaN_Temp_pdoping = 1200; #aim at 1025C surface temp in H2
variable pGaN_Press = 400;#200;
variable pGaN_TMGa_Flow = 5; #40.5/3;
variable pGaN_NH3_Flow = 6000/3;
variable pGaN_Time = 1360; # 70 nm
variable Total_Flow_pGaN = 12000;
variable pGaN_ZnA = 58+5;
variable pGaN_ZnB = 65;
variable pGaN_ZnC = 62;
parameter runtime pGaN_Cp2Mg_source = 200;

Table 2: PGaN/AlGaN/GaN Heterostructure MOCVD Parameters

Here, with these MOCVD recipe parameters, we aimed for the 2DEG AlGaN thickness to be 12.5 nm, the PGaN thickness to be 70 nm, and PGaN hole concentration to be $1 \times 10^{18}\,\mathrm{cm}^{-3}$. Note that this value is not the same as the Mg dopant level, as its ionization energy is about 200 meV, which is quite a high value. At the beginning of our experiment, we were onlhy obsessed with changing parameters in P-GaN layer, whilst leaving the layers underneath as exactly the same as the recipe developed for D-mode HEMT, whose 2DEG AlGaN thickness was 25 nm. If we have such a thick AlGaN thickness, then the 2DEG not only become too far away from the P-GaN, but also the 2DEG density increases. Therefore, the gate fails to suppress the 2DEG at the zero gate-source voltage, and the device remains normally-on even with a highly doped P-GaN layer.

4.2 Mesa Etching (Device Isolation)



(a) Sample before mesa etching

(b) Sample after mesa etching

Figure 9: Mesa etching to leave AlGaN/GaN heterostructure only for active area

Mesa etching(Fig.9) is a step to isolate the active regions of the devices. It was done using OX-35 tool in SNF cleanroom. The possible current path of the PGaN/AlGaN/GaN structure either highly-doped p-type GaN layer or the 2DEG at the AlGaN/GaN interface. If we etch through PGaN and AlGaN, we remove both of them. This step does not require exact etch depth as long as all PGaN and AlGaN are removed for non-active region, and hence overetching is recommended in general. For example, if P-GaN thickness is 60 nm and AlGaN thickness is 20 nm, then the total etch depth should be 80 nm or above. Overetching by 30 60 nm can guarantee the device isolation without problems. Also, since this is the first etching step, this step inscribes the alignment markers for future etchings and metal deposition. This step comprises of two substeps: mesa lithography and mesa etching. **Mesa lithography**(Table.4) is the substep to transfer a pattern on our sample, **mesa etching**(Table.5) is the substep in which the sample goes through actual dry etching.

The table.3 shows the recipes of etching we used. The whole etching step consists of (1) pumping (2) 5-second striking (3) main etching (4) pumping. The BCl_3 gas-based strike step significantly reduces the dead time, where the etching is extremely slow at the beginning due to the oxides on the surface. Since this dead time varies from day to day, from sample to sample, reducing it helps the reproducibility. Characterization of those recipes were done using the AFM tool XE-70 at SNSF.

Between those two recipes, we used the non-selective recipe which etches both AlGaN and GaN with almost the same rate. The mesa etching needs to etch both AlGaN and GaN with fast enough speed. Thus our non-selective etch recipe, which has been being used in X-lab for a long time, could be used here.

Recipe Name	**Strike**	**Selective Etch**	**Non-selective Etch**
Forward Power	150 W	50 W	80 W
ICP Power	250 W	1300 W	250 W
Strike Pressure	20 mTorr	20 mTorr	20 mTorr
APC Set Pressure	10 mTorr	20 mTorr	10 mTorr
He Pressure	7mTorr	7mTorr	7mTorr
Gas	BCl_3 20 sccm Ar 20 sccm	Cl_2 40 sccm N_2 10 sccm O_2 2 sccm	BCl_3 25 sccm Cl_2 10 sccm
PGaN rate	-	70 nm/min	50 nm/min
AlGaN rate	-	4 nm/min	50 nm/min

Table 3: Etching Recipe

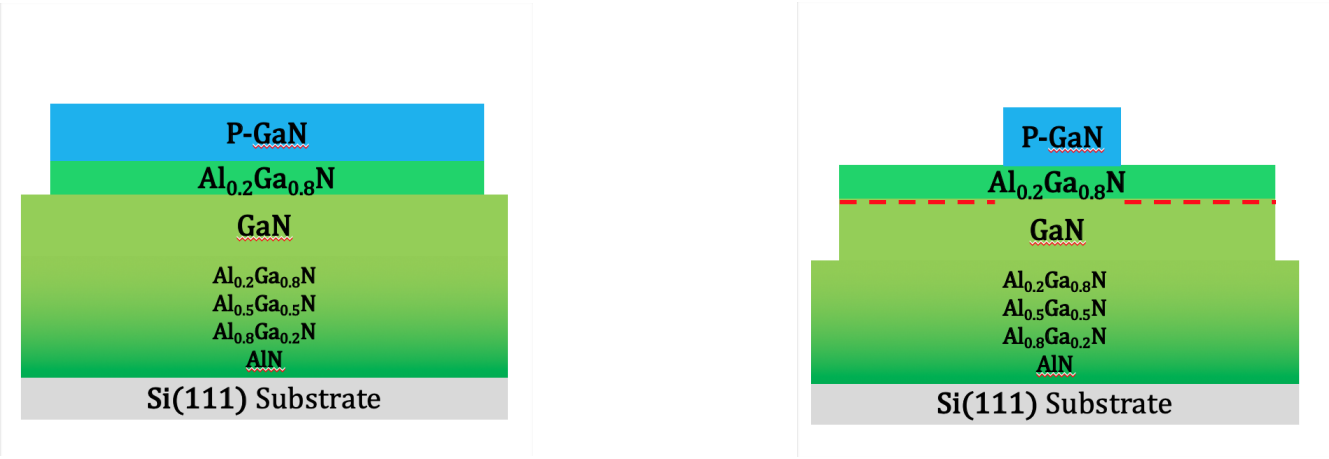
Process Step	Equipment	Temp.	Time	Recipe
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
Blow-drying	wbflexsolv	RT	10 sec	Blow-dry the sample.
HCl Cleaning	wbflexcorr	N/A	20 sec	Clean the sample using diluted HCl (5:1). Dip the sample in the solution which is hot from dilution.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
HDMS	yes	N/A	35 min	Run the pre-set recipe for HDMS coating of the sample.
Photoresist Spinning	headway2	RT	60 sec	Using a 1 um filter and a syringe, drop SPR3612 on top of the sample. Spin it using headway in 5000 rpm for 60 seconds.
Pre-bake	hot plate	90C	1 min	Place the sample on the hot plate.
Exposure	heidelberg	RT	N/A	Expose the sample using the mask for mesa etching. Make sure the mask is inverted, so that the drawn part is protected.
Post-bake	hot plate	115C	1 min	Place the sample on the hot plate.
Development	headway2 bench	RT	30 sec	Prepare two beakers, one filled with DI water and the other filled with MF26A developer. Using a teflon basket, dip the sample in MF26A for 30 seconds, then rinse it using DI water.
Blow-drying	headway2 bench	RT	10 sec	Blow-dry the sample.
Development Check	optical microscope	RT	N/A	Using one of the optical microscopes, check if the photoresist is developed correctly. If not, develop it for additional time. If it still fails, then go back to acetone cleaning.
Hard-bake	hot plate	115C	5 min	Place the sample on the hot plate.

Table 4: Mesa Lithography

Process Step	Equipment	Temp.	Time	Recipe
Etcher Cleaning	ox-35	N/A	15 min	Run recipe "OPT 3-step Clean" to clean inside the etcher chamber. Use a dummy wafer.
Etcher Conditioning	ox-35	N/A	15 min	Run the GaN etching recipe(e.g. "XLab PGaN Y") to condition inside the etcher chamber. Use a dummy wafer.
Etching	ox-35	N/A	Calc.	Dry etch the sample. The duration of etching should be calculated by desired etch depth(t_{PGaN},t_{AlGaN}) divided by the recipe etch rate(r_{PGaN},r_{AlGaN}). The minimum etching time τ_{etch} can be calculated as the sum of $\tau_{PGaN} = t_{PGaN}/r_{PGaN}$ and $\tau_{AlGaN} = t_{AlGaN}/r_{AlGaN}$ (e.g. Assume the PGaN thickness and the AlGaN thickness are 60 nm and 20 nm respectively. Then with "XLab PGaN Y"'s etch rates, namely, PGaN 20 nm/min and AlGaN 20 nm/min, the total etching time is 60/20+20/20 = 4 [min]. We can overetch to about 5 min.)
SRS-100 Cleaning	wbflexcorr	60C	20 min	Clean the sample using SRS-100(N-Methyl-2 Pyrrolidone 60%, Tetramethylen Sulfone 30%, Isopropanolamine 10%). Dip the sample in the solution using a teflon basket. After 20 minutes, dip the sample in DI water for 1 minute and rinse the sample again with flowing DI water.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.

Table 5: Mesa Etching

4.3 P-GaN Etching (Gate Definition)

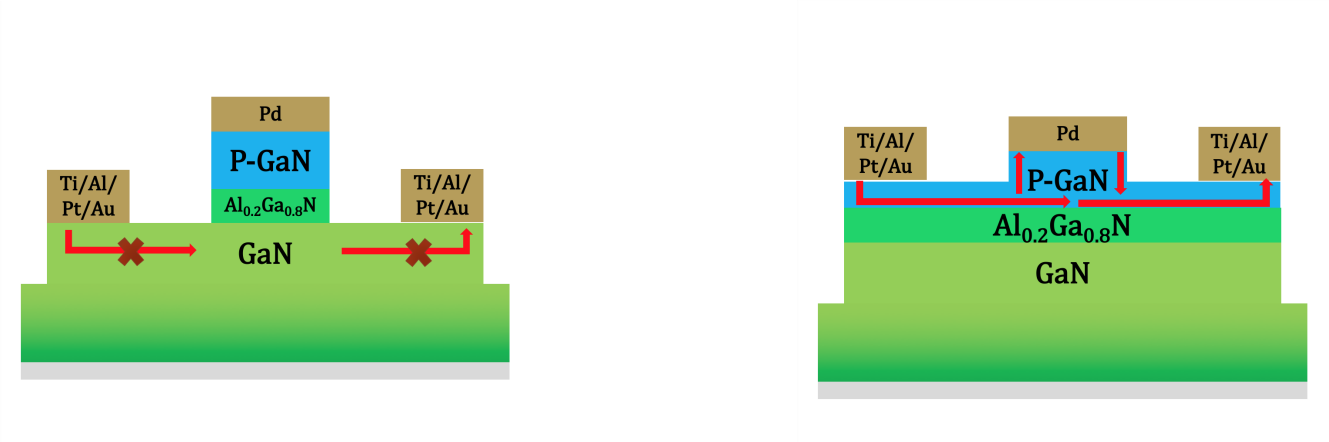


(a) Sample before PGaN etching

(b) Sample after PGaN etching

Figure 10: PGaN etching to leave PGaN layer only for the gate area

PGaN etching(Fig.10) is a step to define the gate areas of the devices. This step removes all the PGaN left after mesa etching, except for the gate area where 2DEG should be normally-suppressed. This step needs to completely remove the P-GaN, but leave the AlGaN layer intact. This is very tricky in our environment, where our shared tool changes the etch rate little by little each day and the dead time variation is still hard to control. Both underetching and overetching can fail the device. Fig.11a shows a device where the overetching removed AlGaN layer. In this case, since the 2DEG of AlGaN/GaN heterostructure is lost and instrinsic GaN is insulating, we have no current path between source and drain. Fig.11b shows when the PGaN is underetched. Since the metal contacts are shorted by the highly-doped p-type GaN layer, the device does not function as a transistor and we see very high gate leakage. (Note that, though the gate is a Schottky contact instead of an Ohmic contact, it does not completely block current flow for positive bias.) Hence we need extremely well-controlled etching. Only about 0-5 nm of overetching is acceptable. For example, if P-GaN thickness is 60 nm, then the total etch depth should be 60-65 nm.



(a) AlGaN layer removed after too much overetching

(b) PGaN layer shorts metal contacts excessive underetching

Figure 11: PGaN etching failure due to erroneous etch depth control.

Hence, the only way to achieve this was to develop a selective etching recipe, which will etch GaN (P-GaN) layer with high rate but will not etch AlGaN. We started from a recipe by Greco et al. wrote in their paper[8], where oxygen gas was used for the etching, which was a very new concept to us. Through lots of trials and errors we developed a recipe as in 3. This recipe etches GaN with the rate of about 70 nm/min. However, this recipe cannot etch AlGaN well, where the rate is only about 4 nm/min. Our hypothesis is that the added O_2 gas with a certain combination of the plasma power and pressure results in an Al_2O_3-like barrier that slows down the etching. (It is a well-known fact that, unlike BCl_3, Cl_2 gas based ICP etching recipes do not etch Al_2O_3 well.) But this is only a hypothesis, which was not thoroughly investigated.

This step comprises of 2 substeps: PGaN test lithography, PGaN test etching, PGaN test, PGaN lithography and PGaN etching. Those are pretty much the same as the mesa etching: **PGaN lithography**(Table.5) and **PGaN etching**(Table.5)

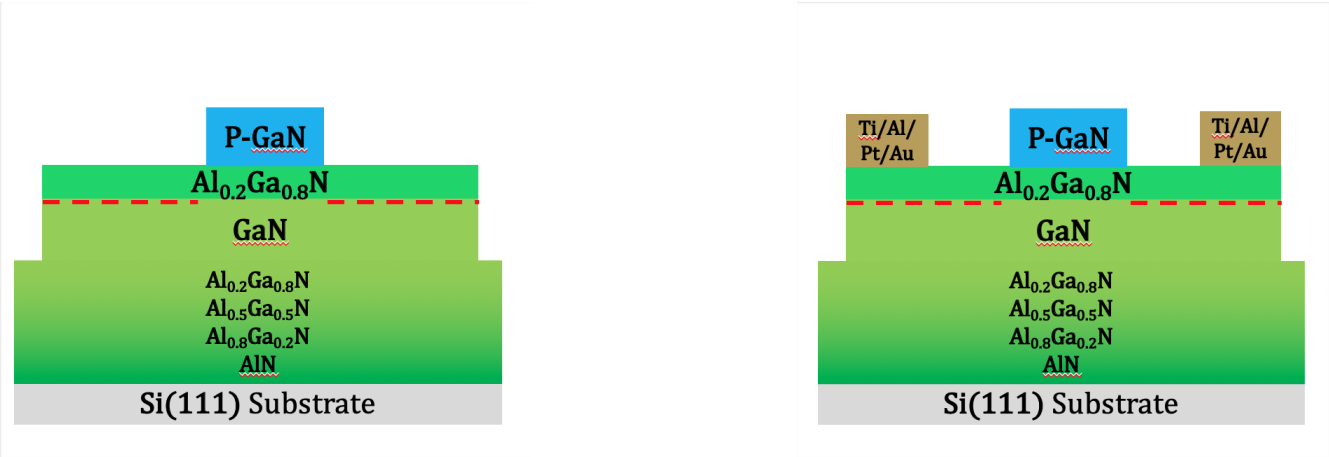
Process Step	Equipment	Temp.	Time	Recipe
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
Blow-drying	wbflexsolv	RT	10 sec	Blow-dry the sample.
HCl Cleaning	wbflexcorr	N/A	20 sec	Clean the sample using diluted HCl (5:1). Dip the sample in the solution which is hot from dilution.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
HDMS	yes	N/A	35 min	Run the pre-set recipe for HDMS coating of the sample.
Photoresist Spinning	headway2	RT	60 sec	Using a 1 um filter and a syringe, drop SPR3612 on top of the sample. Spin it using headway in 5000 rpm for 60 seconds.
Pre-bake	hot plate	90C	1 min	Place the sample on the hot plate.
Exposure	heidelberg	RT	N/A	Expose the sample using the mask for PGaN etching. Make sure the mask is inverted, so that the drawn part is protected.
Post-bake	hot plate	115C	1 min	Place the sample on the hot plate.
Development	headway2 bench	RT	30 sec	Prepare two beakers, one filled with DI water and the other filled with MF26A developer. Using a teflon basket, dip the sample in MF26A for 30 seconds, then rinse it using DI water.
Blow-drying	headway2 bench	RT	10 sec	Blow-dry the sample.
Development Check	optical microscope	RT	N/A	Using one of the optical microscopes, check if the photoresist is developed correctly. If not, develop it for additional time. If it still fails, then go back to acetone cleaning.
Hard-bake	hot plate	115C	5 min	Place the sample on the hot plate.

Table 6: PGaN lithography

Process Step	Equipment	Temp.	Time	Recipe
Etcher Cleaning	ox-35	N/A	15 min	Run recipe "OPT 3-step Clean" to clean inside the etcher chamber. Use a dummy wafer.
Etcher Conditioning	ox-35	N/A	15 min	Run the GaN etching recipe(e.g. "XLab PGaN Y") to condition inside the etcher chamber. Use a dummy wafer.
Etching	ox-35	N/A	Calc.	Dry etch the sample. The duration of etching should be calculated by desired etch depth(t_{PGaN}) divided by the recipe etch rate(r_{PGaN}). The etching time τ_{etch} can be calculated as $\tau_{PGaN} = t_{PGaN}/r_{PGaN}$ We applied 20% over-etching with confidence in the selectivity of the recipe.
SRS-100 Cleaning	wbflexcorr	60C	20 min	Clean the sample using SRS-100(N-Methyl-2 Pyrrolidone 60%, Tetramethylen Sulfone 30%, Isopropanolamine 10%). Dip the sample in the solution using a teflon basket. After 20 minutes, dip the sample in DI water for 1 minute and rinse the sample again with flowing DI water.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.

Table 7: PGaN etch

4.4 Ohmic Contact(S,D) Formation



(a) Sample before Ohmic contact formation

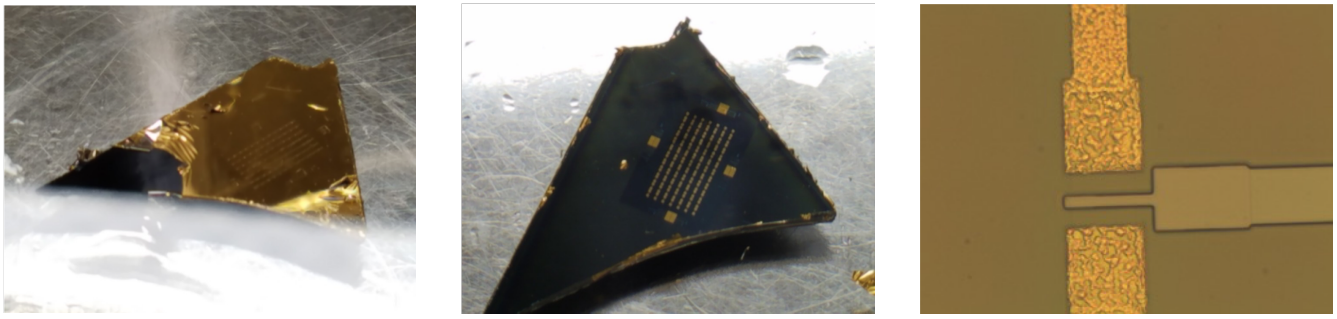
(b) Sample after Ohmic contact formation

Figure 12: Ohmic contacts formed for the source and drain contacts

Now we need to form source and drain contacts(Fig.12). This should be done before the gate contact which is a Schottky contact, as the ohmic contact formation requires a rapid thermal annealing(RTA). The mechanism in which we form an Ohmic contact that connects the metal and the 2DEG underneath the AlGaN layer can be summaraized as following.

First, we deposit Ti(20 nm)/Al(100 nm)/Pt(80 nm)/Au(40 nm). This is done by the infamous lift-off process, in which we coat the sample with photoresist-liftoff dual layer and remove the part for metal deposition. Then we evaporate the metal, then remove the dual layer hence the unwanted metal is removed with the layer. This removal is done by dipping the sample in dedicated solvents(Fig.13a,13b). Then when we heat it at a temperature as high as 850 °C, the formation of TiN and n-type GaN made through the diffusion of Al and N results in an Ohmic contact[10]. You can see the RTA-treated metals in Fig.13c

Therefore, this step consists of 3 substeps, the lithography, the metal evaporation, and the RTA. For metals, in addition to the usual photoresist SPR3612, we use another layer of LOL 2000. This dual layer of lift-off layer/photoresist layer gives a slight undercut during development, and help the metal deposition.



(a) Lift-off process. 24 hours in solvent

(b) Lift-off process completed.

(c) Rapid thermal annealing(RTA)

Figure 13: Lift-off and RTA of Ohmic contacts

Process Step	Equipment	Temp.	Time	Recipe
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
Blow-drying	wbflexsolv	RT	10 sec	Blow-dry the sample.
HCl Cleaning	wbflexcorr	N/A	20 sec	Clean the sample using diluted HCl (5:1). Dip the sample in the solution which is hot from dilution.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
HDMS	yes	N/A	35 min	Run the pre-set recipe for HDMS coating of the sample.
Lift-off Layer Spinning	headway2	RT	30 sec	Using a 1 um filter and a syringe, drop LOL2000 on top of the sample. Spin it using headway in 3000 rpm for 30 seconds.
Lift-off-bake	hot plate	170C	5 min	Place the sample on the hot plate.
Photoresist Spinning	headway2	RT	60 sec	Using a 1 um filter and a syringe, drop SPR3612 on top of the sample. Spin it using headway in 5000 rpm for 60 seconds.
Pre-bake	hot plate	90C	1 min	Place the sample on the hot plate.
Exposure	heidelberg	RT	N/A	Expose the sample using the mask for Ohmic contact. This time the mask is *non-inverted*, so that the drawn part is removed and metal can fill in this vacancy.
Post-bake	hot plate	115C	1 min	Place the sample on the hot plate.
Development	headway2 bench	RT	30 sec	Prepare two beakers, one filled with DI water and the other filled with MF26A developer. Using a teflon basket, dip the sample in MF26A for 30 seconds, then rinse it using DI water.
Blow-drying	headway2 bench	RT	10 sec	Blow-dry the sample.
Development Check	optical microscope	RT	N/A	Using one of the optical microscopes, check if the photoresist is developed correctly. If not, develop it for additional time. If it still fails, then go back to acetone cleaning.
Hard-bake	hot plate	115C	5 min	Place the sample on the hot plate.
De-scum	drytek2	N/A	2 min	Run drytek2 descum recipe for 2 minutes to remove any organics left.

Table 8: Ohmic lithography

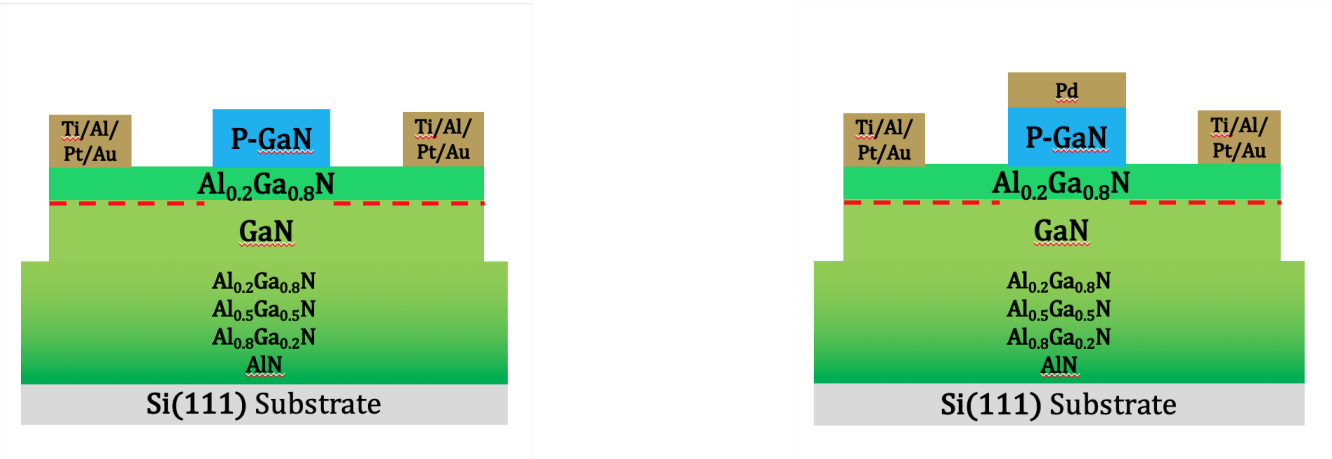
Process Step	Equipment	Temp.	Time	Recipe
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
Evaporation	aja-evap	N/A	N/A	Deposit metals:Ti(20 nm)/Al(100 nm)/Pt(80 nm)/Au(40 nm). Make sure you wait for 10 minutes between each metal deposition.
Lift-off	wbflexsolv	RT	24 hr	Put the sample in a beaker filled with Remover 1165 solvent. Since the metal layer is thick, dipping the sample in the solvent alone might not remove the lift-off layer easily. Peeling off the layer after 24 hours can help.
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
SRS-100 Cleaning	wbflexcorr	60C	20 min	Clean the sample using SRS-100(N-Methyl-2 Pyrrolidone 60%, Tetramethylen Sulfone 30%, Isopropanolamine 10%). Dip the sample in the solution using a teflon basket. After 20 minutes, dip the sample in DI water for 1 minute and rinse the sample again with flowing DI water.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.

Table 9: Ohmic evaporation

Process Step	Equipment	Temp.	Time	Recipe
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
RTA	aw610	850C	30 sec	Recipe:P_850N2 Gas: N_2 10 sccm Ramping: 0C to 850C (20 sec) Steady: 850C (30 sec) Cooling 0C (60 sec)

Table 10: Ohmic rapid thermal annealing

4.5 Schottky Contact(G) Formation



(a) Sample before Schottky contact formation

(b) Sample after Schottky contact formation

Figure 14: Schottky contact formed for the gate

The gate metal deposition(Fig.14) is the last step. Here, we form Schottky contact instead of Ohmic contact. Of course, when positive gate voltage is applied, the Schottky contact cannot block much current. However, it still gives much less gate leakage compared to Ohmic contacts. In general, high-workfunction metals such as Pt or Pd will do. Here we used the Pd. The procedure is pretty much the same as Ohmic contact, however, this time we only deposit 50 nm of Pd metal and do not perform any RTA.

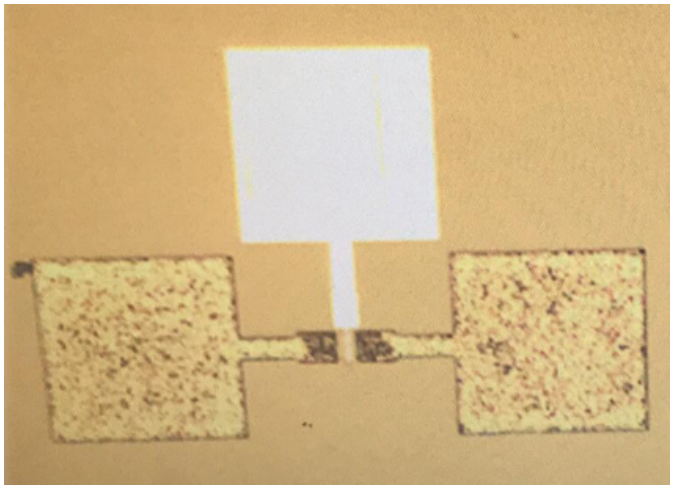


Figure 15: Schottky contact formed(white metal)

Process Step	Equipment	Temp.	Time	Recipe
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
Blow-drying	wbflexsolv	RT	10 sec	Blow-dry the sample.
HCl Cleaning	wbflexcorr	N/A	20 sec	Clean the sample using diluted HCl (5:1). Dip the sample in the solution which is hot from dilution.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
HDMS	yes	N/A	35 min	Run the pre-set recipe for HDMS coating of the sample.
Lift-off Layer Spinning	headway2	RT	30 sec	Using a 1 um filter and a syringe, drop LOL2000 on top of the sample. Spin it using headway in 3000 rpm for 30 seconds.
Lift-off-bake	hot plate	170C	5 min	Place the sample on the hot plate.
Photoresist Spinning	headway2	RT	60 sec	Using a 1 um filter and a syringe, drop SPR3612 on top of the sample. Spin it using headway in 5000 rpm for 60 seconds.
Pre-bake	hot plate	90C	1 min	Place the sample on the hot plate.
Exposure	heidelberg	RT	N/A	Expose the sample using the mask for Schottky contact. This time the mask is *non-inverted*, so that the drawn part is removed and metal can fill in this vacancy.
Post-bake	hot plate	115C	1 min	Place the sample on the hot plate.
Development	headway2 bench	RT	30 sec	Prepare two beakers, one filled with DI water and the other filled with MF26A developer. Using a teflon basket, dip the sample in MF26A for 30 seconds, then rinse it using DI water.
Blow-drying	headway2 bench	RT	10 sec	Blow-dry the sample.
Development Check	optical microscope	RT	N/A	Using one of the optical microscopes, check if the photoresist is developed correctly. If not, develop it for additional time. If it still fails, then go back to acetone cleaning.
Hard-bake	hot plate	115C	5 min	Place the sample on the hot plate.
De-scum	drytek2	N/A	2 min	Run drytek2 descum recipe for 2 minutes to remove any organics left.

Table 11: Schottky lithography

Process Step	Equipment	Temp.	Time	Recipe
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.
Evaporation	aja-evap	N/A	N/A	Deposit metals:Pd(50 nm).
Lift-off	wbflexsolv	RT	24 hr	Put the sample in a beaker filled with Remover 1165 solvent. Since the metal layer is thick, dipping the sample in the solvent alone might not remove the lift-off layer easily. Peeling off the layer after 24 hours can help.
Acetone Cleaning	wbflexsolv	RT	10 min	Dip the sample in acetone for 10 minutes.
Methanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with methanol for 10 seconds.
2-prophanol Cleaning	wbflexsolv	RT	10 sec	Spray the sample with 2-propanol for 10 seconds.
SRS-100 Cleaning	wbflexcorr	60C	20 min	Clean the sample using SRS-100(N-Methyl-2 Pyrrolidone 60%, Tetramethylen Sulfone 30%, Isopropanolamine 10%). Dip the sample in the solution using a teflon basket. After 20 minutes, dip the sample in DI water for 1 minute and rinse the sample again with flowing DI water.
Blow-drying	wbflexcorr	RT	10 sec	Blow-dry the sample.
Dehydration	hot plate	90C	3 min	Place the sample on the hot plate.

Table 12: Schottky evaporation

5 Analysis

5.1 PGaN Layer Growth Rate/Etch Rate and AlGaN Etch Rate

MOCVD growth of layers(Fig.8) is a significantly important step, as if we do not grow AlGaN and PGaN layers properly, we might completely lose 2DEG instead of suppressing it. Growth of $Al_xGa_{1-x}N$ and GaN has been done at Stanford for years. Therefore we have confidence in having reasonable control over those layers' thicknesses. However, Mg-doped GaN is relatively new, with different temperature, pressure etc. Therefore, understanding the PGaN growth including the growth rate as well as the doping level was very important.

To confirm the thicknesses of the grown layer in the MOCVD, we used the SEM. Using Dr Xu's help, we cleaved a small piece with the whole PGaN/ AlGaN/GaN layers grown. The cleaved piece was then put vertically in the SEM (FEI Serion) and we performed a cross-sectional SEM. The fig.16 shows the SEM images of PGaN for different growths.

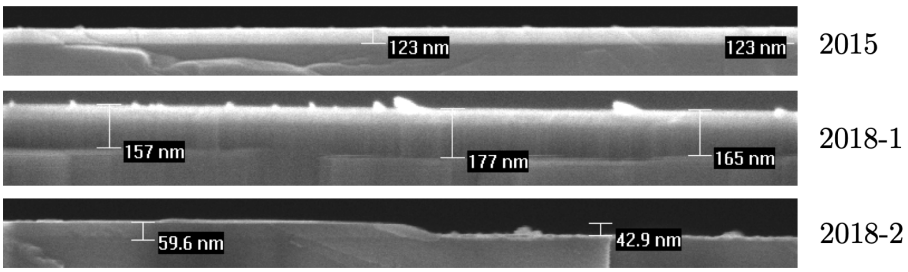


Figure 16: PGaN thickness measured at different times.

With PGaN having much higher conductivity, the SEM images are supposed to clearly show the boundary between PGaN the rest of the layers with good contrast in the colors. AlGaN layer cannot be seen as it is only about 25 nm thick.

Later, those P-GaN thickness as well as the P-GaN growth rate could be confirmed by using our selective etching recipe. We grew sample with P-GaN on top of AlGaN, then we applied our selective etching recipe for a while. With different etch time, we got different etch depths, and by solving a system of equations we could find out the P-GaN etch rate, then the thicknesses of the P-GaN and AlGaN layers. Due to the existence of the dead time, those solutions might not be very accurate. But given that the tool performance changes from time to time for those shared equipments, the values we found were acceptable, and fabrication of the E-mode HEMTs based on those numbers was successful.

5.2 PGaN Layer Electrical Property Analysis

From the P-GaN/AlGaN/GaN structure, we performed the hall measurement to verify whether the 2DEG is suppressed by the P-GaN layer. Using the full model for the hall effect when both the electrons and the holes matter, the Hall coefficient can be written as

$$R_H = \frac{1}{e}\frac{-n\mu_n^2 + p\mu_p^2}{(n\mu_n + p\mu_p)^2} \tag{5}$$

and we know that the total conductivity can be calculated as

$$\sigma_{tot} = \sigma_n + \sigma_p = en\mu_n + ep\mu_p \tag{6}$$

These are 2 equations with 4 variables, the electron mobility μ_n, the electron density n, the hole mobility μ_p and the hole density p. Usually, we ignore one of the carriers and get the mobility and the density of the other carrier. But instead, we can assume the mobility values to be typical values and calculate the densities of both carriers. With the assumption of $\mu_n = 1200\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ and $\mu_p = 10\,\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, we could find that

$$n_{_{2DEG}} \approx 1 \times 10^{10}\,\mathrm{cm}^{-2}$$
$$p_{_{PGaN}} \approx 1 \times 10^{18}\,\mathrm{cm}^{-3}$$

Without additional treatment such as P-GaN cap layer, the typical value of the 2DEG electron sheet density is about $1 \times 10^{13}\,\mathrm{cm}^{-2}$. We saw an approximately 1,000 times decrease in 2DEG density for zero bias. Therefore, we could conclude that a thick enough P-GaN cap can actually suppress the 2DEG to make the device e-mode.

Later, we grew a thick P-GaN on a sapphire substrate to separate P-GaN from the AlGaN/GaN 2DEG and measure. The result showed that

$$\mu_{_{PGaN}} \approx 3.92\,\mathrm{cm}^2/\mathrm{Vs}$$
$$p_{_{PGaN}} \approx 9.16 \times 10^{17}\,\mathrm{cm}^{-3}$$

This means our previous analysis was reasonably accurate.

6 Device Measurement

Figure 17: Optical microscope images of the finished devices

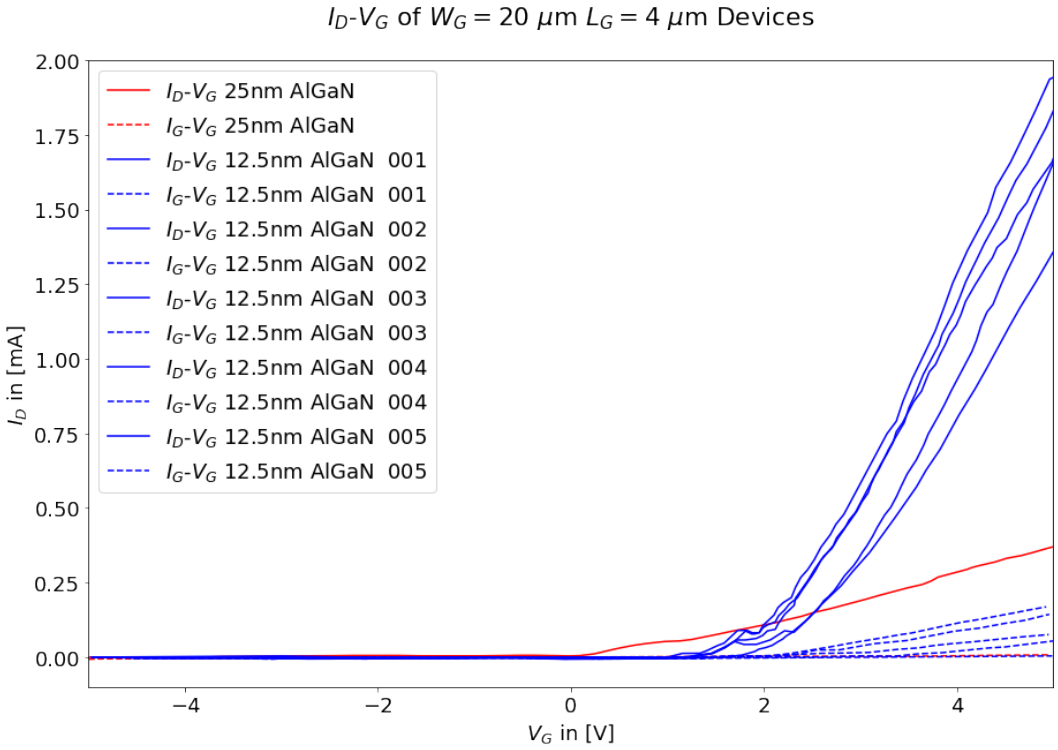


Figure 18: $I_D - V_G$ and $I_G - V_G$ curves or our 20 μm width devices. $V_{DS} = 5$ V. The original data csv files were lost, so those data were retrieved from the pictures of the plots taken during the measurement with graph-reading applications.

In Fig. 18, we have the measurement data from 6 devices total. The red line is the measurement data from

P-GaN HEMT with 2DEG AlGaN thickness 25nm. On the other hand, the other five devices with blue-colored plots are the ones with 12.5 nm AlGaN. Note that the threshold voltage improved a lot when the AlGaN thickness was reduced. It is unclear why the 25nm devce has lower current than the 12.5nm devices, as theoretically the 2DEG density should be much higher in the 25 nm devices. There is a possibility that the RTA or any other process did not go well on that specific sample.

Aside from the threshold voltage, there are two more things things we can pay attention to about the 25 nm AlGaN devices. The first thing is a weird "kink" at the beginning of the device turn-on. When the gate-source voltage was between +1 V to +2 V, we see the devices starting to turn on. But instead of monotonically increasing as we usually see from other FETs, we see a couple of ups and downs of the drain current. After a short period of those, eventually the drain current begins to monotonically increase as the gate voltage increases. Our hypothesis was that increased electric field within the P-GaN region changes the activation status of the Mg dopants inside, however, this is not proven by any additional experiments. Interestingly, 1 out of 5 devices (Device 001) in the Fig. 18 showed regular monotonically increasing curve as expected. Therefore, those kinks might be just coming from the imperfection of our fabrication process for those experimental devices.

The other thing notable is a quite high gate leakage. Except for one device (Device 002), we see high gate currents which is only 1 2 orders of magnitudes lower than the drain current. We are conjecturing that, without any passivation layer between the GaN layer and the gate metal, there is a small region where the gate metal touches the 2DEG (Fig. 7. The Schottky metal that is connecting the gate and the gate pad can touch the 2DEG exposed on the sides. Therefore, for a more rigorous device, we need to passivate the device with oxides before gate deposition. Then we can make a via hole on top of gate and deposit gate metal. If we change the process in this way, we expect to see much smaller gate leakage that is several orders of magnitudes lower than the drain current.

Unfortunately, we do not have the data for the $I_D - V_D$ measurements. Even though I performed the measurement, I did not save the data, as I decided to work on another sample with passivation, as the aforementioned gate leakage was not satisfactory. However, after that I had to start focusing on my other projects as I moved my group, and later the COVID19- related shut down of the lab along with my bad inventory habit at that time lost the fabricated sample.

After the shutdown was over and the SNF began to operate again, Dr. Xiaoqing Xu and I discussed whether we would make another device for the measurement, not only to improve the performance by adopting the passivation layer but also by changing the P-GaN properties such as doping level or thickness. However, as we ran out of our originally proposed budget as will be mentioned in the following section, and I had to focus on other projects after changing the group, we finally decided to stop the project, as our main goal of finding a recipe for a working e-mode HEMT was achieved.

7 Financial Report

Since we struggled a lot in the MOCVD process, our expenditure exceeded our proposed amount by $1,111, and this is one of the main reasons we stopped our project in the middle though we did not reach all the goals initially proposed. MOCVD expenses for the tool troubleshooting for the cracking issues were exempted.

	SNF Expense($)	MOCVD Expense($)	nSiL Expense($)	Total ($)
Proposed Budget	4590	3200	1800	9590
MOCVD Troubleshooting 0	9168	0	9168	
Expenditure Before Extension	3070	12458	1155	16683
Expenditure After Extension	823	1855	508	3186
Expenditure for Project	2149	5145	646	7940
Remaining Budget	697	-1945	137	-1111

8 Conclusion & Future Work

This project indeed started a long time ago, as its origin was our ENGR241 project. And finally we got a working device. We have confirmed that the 2DEG AlGaN thickness played a key role in suppressing the 2DEG with P-GaN, and developed a good selective etching recipe that freed us from the horror of under-etching or over-etching problem. We ended up with a full process run sheet for this device.

However, my bad inventory habit along with the abrupt lab shutdown due to COVID19 lost our samples and the full characterization of the fabricated devices did not happen. Moreover, many external factors such as lab switching, budget limit, and stopped us from continuing on our other goals proposed. These failures helped me developing better management skills on setting practical goals, maintaining the samples, etc.

And all the things we could not finish can be possible future topics for the ENGR241 class project or a community service project, if any student or SNF/SNSF staff is interested in P-GaN E-mode HEMT as a topic. For example, they can try to make devices with proper passivation as mentioned above to make "complete" devices. Then, by using de-embedding structures they can measure the RF performance of those devices. Since E-mode HEMTs are of interest in power fields as well, measuring the breakdown characteristic can also be useful. If anybody from Stanford X-lab or anybody interested in extreme-environment electronics would take over this project, they can try measuring the devices in high-temperature or even high-radiation environment. Lastly, changing the P-GaN properties and analyzing how it affects the device performance will give people a valuable piece of information. However, due to the limited budget in ENGR241 classes, this P-GaN analysis requiring multiple MOCVD growth might not be practical.

Overall, it was a painful but meaningful and fun experience. Though not all of our goals were achieved, whatever achievement I made here came from endless support of people in X-lab and SNF. I want to thank everybody, especially Dr. Xiaoqing Xu, who has been an amazing mentor. I wish her the best luck with her new journey in a new environment.

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