ALD Oxide Nanolaminates Final Presentation

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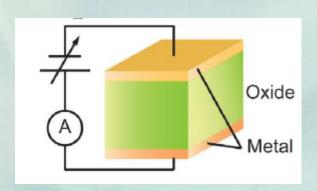
Mentor: J Provine

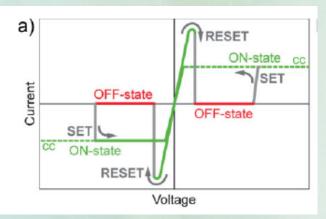
Outline

- Motivation
- Overall Schedule
- Device Fabrication
- Measurement & Discussion
 - Growth Thickness
 - Leakage Current
 - Breakdown Voltage
 - RRAM Characteristics
- Summary

Motivation (1)

- Resistance random access memory(ReRAM) application
 - A ReRAM memory cell is a capacitor-like structure composed of insulating or semiconducting transition metal oxides that exhibits reversible resistive switching on applying voltage pulses [1]
 - Plenty of transition metal oxides have such property: HfOx [2], AlOx [3], NiO, TiOx, WOx, CuOx, etc.





[1] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-Based Resistive Switching Memories – Nanoionic Mechanisms, Prospects, and Challenges," *Adv. Mater.*, vol. 21, pp. 2632-2663, 2009.

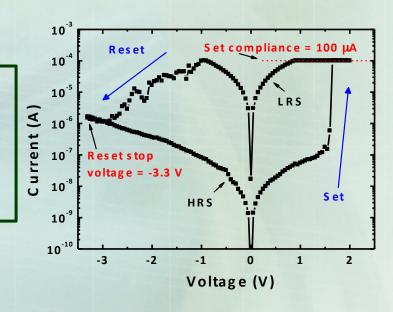
[2] H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, C. H. Lien, and M. J. Tsai, "Low Power and High Speed Bipolar Switching with A Thin Reactive Ti Buffer Layer in Robust HfO2 Based RRAM," in *IEDM Tech. Dig.*, 2008, pp. 297-300.
[3] Y. Wu, B. Lee, and H. S. P. Wong, "Al2O3-Based RRAM Using Atomic Layer Deposition (ALD) With 1-μA RESET Current," *IEEE Electron Device Letters*, vol. 31, pp. 1449-1451, 2010.

Motivation (2)

- Savannah to deposit HfOx/AlOx nanolaminates for RRAM devices, aiming to achieve lower switching power and better switching uniformity and reliability.
- Oxide property extraction, e.g. leakage current, breakdown voltage from MIM structures

I-V curve from TiN/HfOx/AlOx/Pt RRAM devices

* The oxide laminate was deposited at Cambridge Nanotech using Fiji system



Overall Timetable

| Week | Job Description |
|------|--|
| 1-2 | Start of the quarter; training of the equipment tool including Savannah/ woollam/ wetbench-diff/ innotec, etc. |
| 3-4 | ALD AlOx deposit with 3nm/5nm/10nm thickness on Si/TiN and Si control wafers at 200°C using standard recipe |
| 5 | ALD HfOx deposit with 3nm/5nm/10nm thickness on Si/TiN and Si control wafers at 200°C using standard recipe |
| 6 | ALD AlOx deposit with 100 cycles (target 10nm thickness) on Si/Ti and Si control wafers at 100/150/200/250°C using standard recipe |
| 7 | ALD HfOx deposit with 100 cycles (target 10nm thickness) on Si/Ti and Si control wafers at 100/150/200/250°C using standard recipe |
| 8 | (1) ALD HfOx at 100/150/200/250°C targeted at same thickness (~10nm); (2) ALD AlOx/HfOx lamninate deposition: AlOx/HfOx bilayer |
| 9 | Summary |

Device Fabrication

50mmTIN (CAVPIDON) Highly-doped Si Highly-doped Si TE Pt Patterning (Lift-off) ALD oxide (AlOx, HfOx) Highly-doped Si Highly-doped Si

Measurement Method

1. Thickness (Woollam)

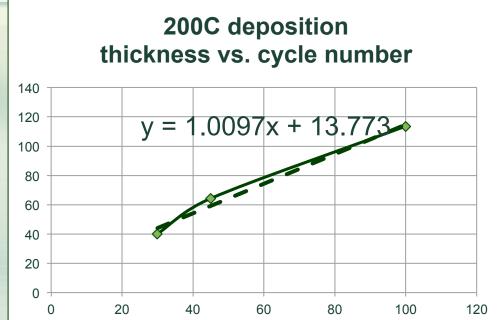
2. Breakdown Voltage

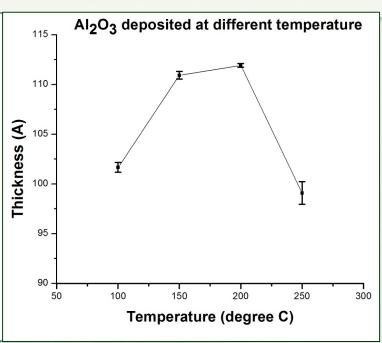
- Oxide immediate breakdown occurs when the current density through the oxide becomes high enough to cause thermal runaway.
- Ramp-up MIM two-terminal voltage up to 10V and extract voltage node at sudden substantial current jump.
- Average 25 points per wafer

3. Leakage Current

- Leakage current suggests the oxide quality, dense degree, etc.
- Extract the initial leakage current before the dielectric breakdown at
 1V
- Average 25 points per wafer

Thickness-ALD AlOx

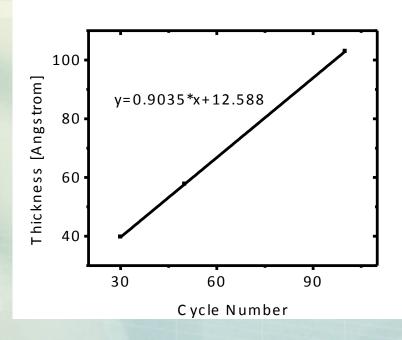


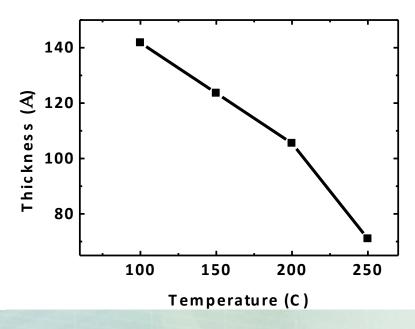


| cycles | Thickness(A) |
|--------|--------------|
| 30 | 40.057 |
| 45 | 64.309 |
| 100 | 113.65 |

| | Mean (A) | STD (A) |
|-------|----------|---------|
| 100 C | 101.67 | 0.48576 |
| 150 C | 110.92 | 0.38361 |
| 200 C | 111.93 | 0.18846 |
| 250 C | 99.085 | 1.1394 |

Thickness-ALD HfOx

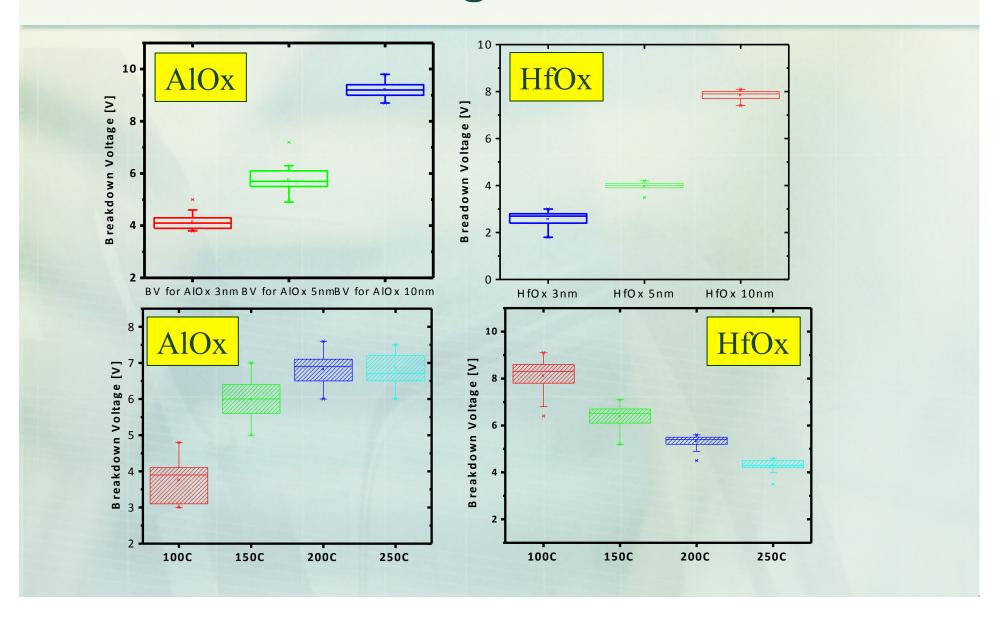




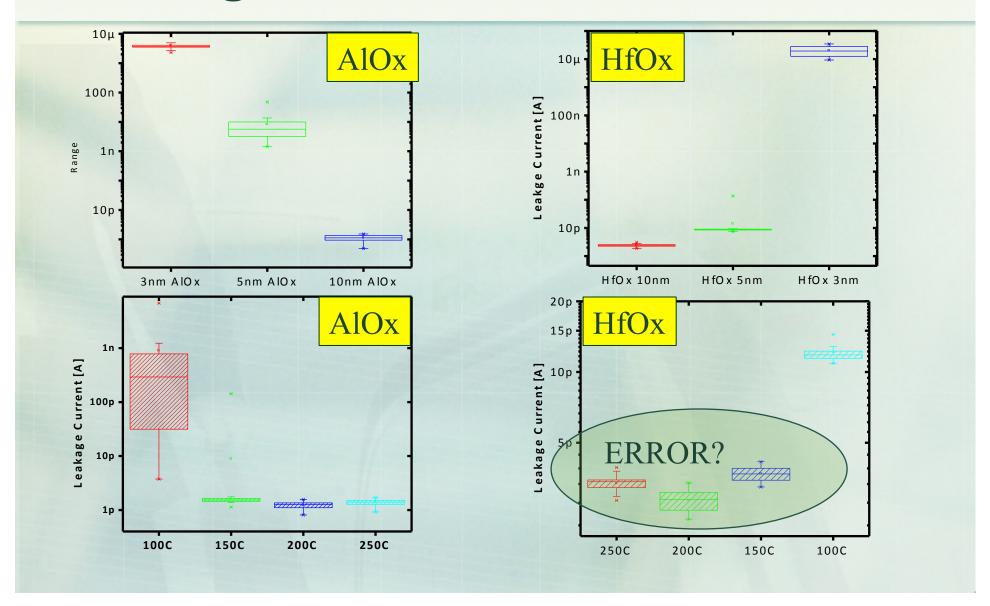
| Cycles | Mean (A) | STD (A) |
|--------|----------|---------|
| 30 | 141.8 | 0.49 |
| 50 | 123.6 | 0.23 |
| 100 | 105.5 | 0.46 |

| Temp | Mean (A) | STD (A) |
|--------|----------|---------|
| 100 °C | 141.8 | 0.49 |
| 150 °C | 123.6 | 0.23 |
| 200 °C | 105.5 | 0.46 |
| 250 °C | 71.0 | 0.33 |

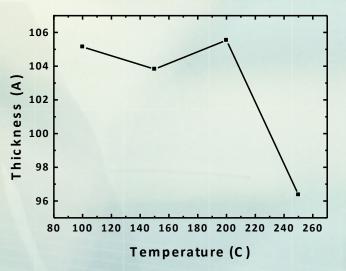
Breakdown Voltage



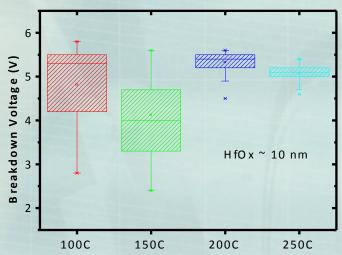
Leakage Current

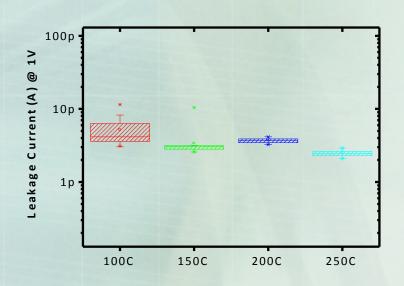


HfOx Quality vs. Temp



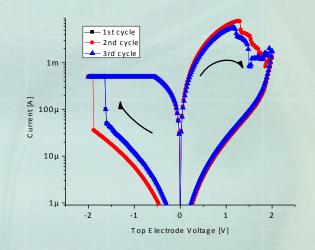
| Temp (C) | Cycle | Thickness (A) |
|----------|-------|---------------|
| 100 | 70 | 105.1472 |
| 150 | 80 | 103.8288 |
| 200 | 100 | 105.5418 |
| 250 | 140 | 96.3694 |





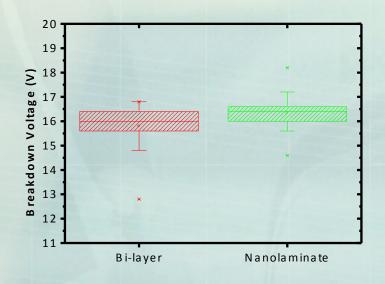
Resistance Switching Characteristics

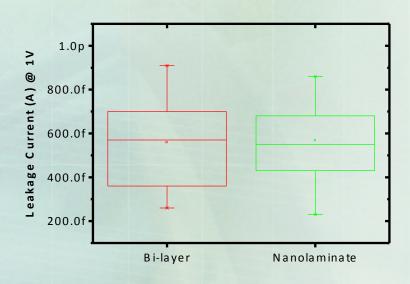
- Few of the devices show the resistance switching behavior but the devices failed after a few cycles
- Reasons: 1) Electrode material; 2)Large dimensions;
 3)Oxide deposition method, etc.
- Solutions: 1) Nanolaminate or bi-layer; 2) Migrate to Fiji system



Bi-layer and Nanolaminate

- Bi-layer: Ti/AlOx(5nm)/HfOx(5nm)/Pt stack
- Nanolaminate: Ti/HfAlOx/Pt stack
- None of the resistance switching phenomenon





Summary

- Fabricate 100μm² MIM structures for RRAM application
- Investigate ALD AlOx and HfOx deposition rate, breakdown voltage and leakage current of oxide films at different temperatures
 - The oxide quality degrades with the temperature decreases
 - The deposition rate of HfOx decreases with temperature increases
 - The breakdown voltage are generally much higher than thinner films
- Bi-layer AlOx/HfOx and Nanolaminate HfAlOx were deposited