Community service project (Jan-Mar 2018)

Characterizing ALD HfO_2 based on different deposition conditions

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MOTIVATION

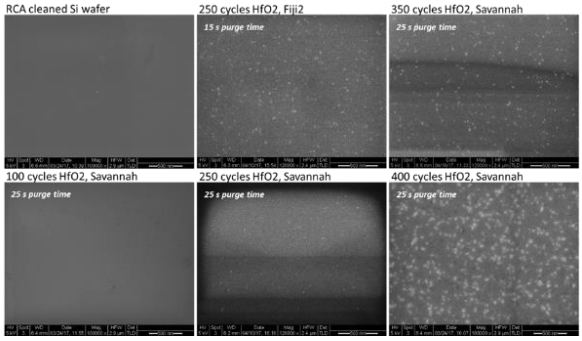


Fig. 1: SEM of ALD HfO2 films deposited at 200 °C

Recently, users have reported observing roughness in the form of 'hillocks' in thicker (> 20 nm) films deposited thermally in Fiji2 and Savannah at 200 °C. The hillocks seem to increase in size and density with the number of ALD cycles. Initial speculation is that they are nanocrystallites which nucleate over the long period of deposition, in spite of the low ALD temperature. This is surprising, as thin films of ALD HfO2 are expected to be amorphous at this temperature. Notably, the purge time between successive ALD cycles was increased from 15 s to 25 s around October 2015 to encourage self-limited growth, effectively increasing the process time by > 60%. It would be useful to see how film morphology varies with process time and temperature, as well as how it affects electrical properties. Amorphous layers are generally preferred for gate oxides due to lower leakage, although polycrystalline films may also be acceptable, and generally have the advantage of higher density and higher dielectric constant. Provided the resulting film is relatively smooth, polycrystalline films could still be used in capacitive applications if the crystallites in the film are much smaller than the film thickness so that grain boundaries do not extend through the thickness of the film, or if grain sizes are large and predictable relative to device feature size.

There are several studies in the literature that touch on the evolution of texture in ALD HfO2 films with temperature and film thickness. Gieraltowska *et al* report on a low temperature (T_g = 85 °C) recipe for HfO2 in the Savannah reactor, with TDMAH and DI water precursors and a purge time of 10 s. Table 1 shows the comparison of electrical properties of MOS structures based HfO2 thickness between 20 and 200 nm, deposited at 85 °C. In this case, the HfO2 films of thickness 100 nm and below were amorphous, with smooth surfaces (RMS roughness ~ 0.5 nm), and much lower leakage current and higher breakdown electric field than the crystalline film that developed at a thickness of 200 nm. At T_g = 135 °C, only the thinner films (20, 40 nm) were amorphous, and the 100 nm thick film was polycrystalline. The effect of deposition temperature on MOS capacitors formed with 100 nm thick films is shown in Table 2. As T_g increased, the degree of crystallinity, and consequently leakage current, dielectric constant and RMS roughness increased while dielectric strength decreased.

Table 1 (T_g = 85 °C)

Electrical properties and RMS roughness values of HfO_2 gate dielectrics grown at LT for five different thicknesses of insulator layers.

Thickness [nm]	Dielectric strength [MV/cm]	Leakage current at 1 V [A/cm^2]	Dielectric constant $k \pm 3$	RMS [nm]
200	0.6	$3*10^{-3}$	22	6.0
100	1.3	$2*10^{-6}$	21	0.5
80	1.2	$2*10^{-6}$	19	0.6
40	1.2	$8*10^{-5}$	15	0.4
20	1.0	$6*10^{-5}$	14	0.3

Table 2

Electrical properties and RMS roughness values of HfO_2 gate dielectrics grown at four different temperatures (T_G).

T_G [°C]	Dielectric strength [MV/cm]	Leakage current at 1 V [A/cm^2]	Dielectric constant $k \pm 3$	RMS [nm]
350	0.6	$2.4*10^{-3}$	18	2.9
200	0.6	$3.2*10^{-3}$	18	3.0
135	1	$8.2*10^{-4}$	17	1.6
85	1	$4.9*10^{-6}$	17	1.0

Fig. 2: The XRD determination of percent crystallinity as a function of deposition temperatures for 100 nm-thick hafnium and zirconium oxide films.

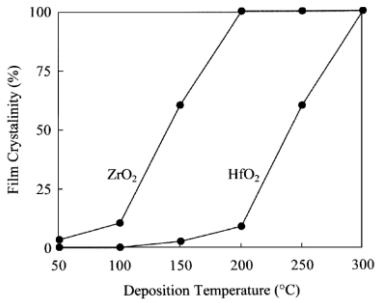
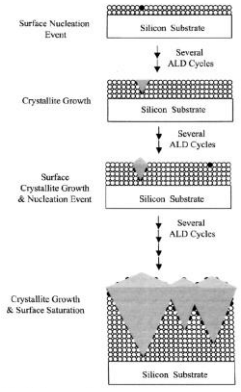


Fig. 3: Proposed crystal growth and nucleation model



Aarik *et al* deposited HfO2 films ranging from 30 – 375 nm using HfCl4 and DI water precursors, and a 2 s purge time. XRD and RHEED measurements demonstrated that films grown at 225 °C were amorphous, while polycrystalline films were obtained at 300 °C and higher, although at 300 °C the crystalline phase only appeared when more than 200 cycles were applied. The crystallite sizes were also observed to depend on the substrate material, being somewhat larger in the films grown on single-crystal silicon than in those grown on fused silica substrates. Hausmann *et al* deposited 100 nm thick HfO2 and ZrO2 films using TDMAH and TDMAZr at temperatures ranging from 50 °C to 300 °C, with 5 s purge time. For both materials, the degree of

crystallinity increased with temperature, as seen in Fig 2. HfO2 films deposited at 100 °C and below were found to be amorphous. TEM studies of 50 nm films revealed spherical and evenly distributed crystalline regions, which were correlated with roughness due to conical features in the AFM images. The roughness reached 5% of the film thickness for films deposited at 150 – 250 °C. Based on these observations, the authors proposed a nucleation and growth model for the ALD films starting with surface crystallite formation and faster vertical and radial growth of the crystallites compared to the surrounding amorphous material (Fig. 3). At higher growth temperatures, nucleation events become more probable and so films become more crystalline. For thicker films (> 100 nm), crystallinity starts to be observed at lower deposition temperatures because the longer process time allows more nucleation events and crystal growth to happen.

Kim *et al* found that ultrathin (3 nm) HfO2 films deposited at 300 °C were mostly amorphous, with sparsely distributed nanometer-sized crystallite 'seeds', but that significant crystallization resulted after a 30 minute anneal at 500 °C. Ho *et al* studied how annealing affects the degree of crystallinity of 20 nm thick HfO2 films deposited on p-Si substrates with a thin interfacial SiO2 layer grown either thermally or chemically (by rinsing wafers with O_3-enriched DI water). The ALD deposition was done with HfCl4 and DI water as precursors, at 300 °C. The HfO2 film deposited on thermal oxide was found to contain columnar grains of ~8 nm width, while the as-deposited film on the chemical oxide was mostly amorphous, though HRTEM imaging suggests short-range order on the sub-nanometer scale.

In his 2015 EE 412 report, Kirby Smithe described measurements done on MOSCAP devices made with ~10 nm of ALD HfO2, and a 15 s purge time. The Savannah depositions were done at 200, 150 and 100 °C and annealed in forming gas at 50 °C above deposition temperature, while the MVD depositions were done at 125 and 100 °C, and annealed at the same temperature.

Overall, the degree of crystallinity of the ALD HfO2 films seems to depend strongly on film thickness and deposition temperature, with some effect from the substrate. For *thin films* (< 40 nm) literature evidence suggests a deposition temperature of 200 °C should result in a mostly amorphous film (with similar ALD conditions, e.g. purge time), while crystallinity starts to be observed in as-deposited films around 250 – 300 °C. The effect of purge time has yet to be reported.

OBJECTIVES

To characterize the effect of 1) Deposition temperature, 2) Purge time and 3) Film thickness on the morphology and electrical properties of HfO2 films deposited in Savannah, before and after annealing. Deposition quality (thickness, uniformity, etc) was also monitored.

SPLITS (include 50 cycles of HfO2 conditioning before each deposition)

1. 5 cycles Al2O3, **200 cycles HfO2**, 200 °C, 25s purge time
2. 5 cycles Al2O3, **300 cycles HfO2**, 200 °C, 25s purge time
3. 5 cycles Al2O3, **400 cycles HfO2**, 200 °C, 25s purge time
4. 5 cycles Al2O3, 200 cycles HfO2, 200 °C, **15s purge time**
5. 5 cycles Al2O3, 400 cycles HfO2, 200 °C, **15s purge time**
6. 5 cycles Al2O3, 200 cycles HfO2, **100 °C**, 25s purge time
7. 5 cycles Al2O3, 400 cycles HfO2, **100 °C**, 25s purge time

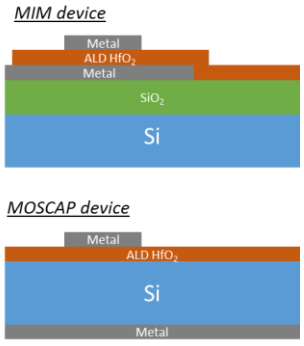


Fig. 1

SAMPLE PROCESSING

Each deposition included a wafer for MIM devices, and another for MOS devices (cross sections shown in Fig. 1). A range of electrode sizes were patterned ranging from 10 µm to 200 µm in diameter, which would allow extraction of both intrinsic normalized capacitance and parasitic capacitance from the capacitance-area plot.

MIM devices	***MOS devices***	***Time***	***Day***
• SC1 clean → SC2 clean (15 wafers)	• -	1 h	1
• Grow 300 nm thermal oxide	• -	6 h	1
• *Measure oxide thickness with Woollam*	• -	0.5 h	1
• Photolithography to define 9-point testing sites (9)	• -	2 h	2
• Deposit 5 nm Ti, 50 nm Pt as bottom electrode	• -	3 h	2
• Liftoff to remove metal from 9-point testing sites	• SC1 clean → SC2 clean → HF dip	Overnight	3-9
• ALD deposition → *measure film thickness*	• ALD deposition → *measure film thickness*	**4 – 6 h (x7)**	3-9
• Photolithography to define top electrodes	• Photolithography to define top electrodes	2 h	10

• Deposit 5 nm Ti, 70 nm Pt or top electrodes • Liftoff • - • Cleave wafer in half • Anneal half of wafer • - • *Characterize electrical properties of devices* • *Characterize structural properties of devices*	• Deposit 5 nm Ti, 70 nm Pt or top electrodes • Liftoff • Scratch backside oxide, deposit backside metal • Cleave wafer in half • Anneal half of wafer • *Characterize electrical properties of devices* • Dice wafer to obtain samples for XRD and SEM • *Characterize structural properties of devices*	3 h Overnight 3 h 0.5 h 0.5 h 12 h 3 h 5 h **Total time:** ~ 90 h	10 10 11 11 11 12 14 15 ~3 wks

The devices were laid out on the wafers such that areas will be left 'empty', allowing a 9-point thickness measurement to be done to estimate deposition uniformity. This can be seen as the dark spots in Fig. 2. The grid of 1 mm squares indicates the positions individual devices. Half of the wafer was annealed while the other half was kept unannealed. Fig. 3 shows the placement of the device-carrying wafers and carrier half-wafers in the ALD chamber.

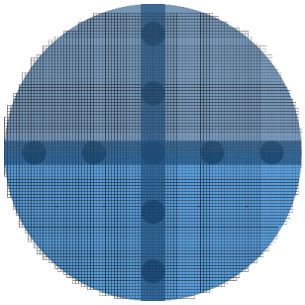


Fig. 3: Rough layout of individual wafer

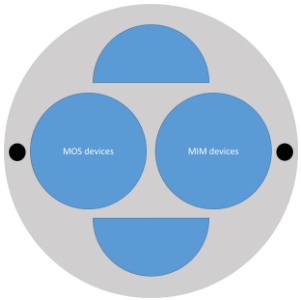


Fig. 4: Placement of wafers in ALD chamber

CHARACTERIZATION

Morphology:

- Woollam thickness measurement
- SEM imaging to visualize size and density of nanocrystallites (if present)
- AFM to characterize surface roughness
- XRD to characterize degree of crystallinity

Electrical characteristics:

- Leakage current and capacitance density can be obtained from MIM devices
- Capacitance density can also be measured from MOSCAP devices

TOOLS & MATERIALS

Device fabrication tools:

- Wbclean, wbsolv
- Thermco1
- Innotec (2 depositions)
- Savannah (7 depositions)
- Tylan9
- Svgcoat, Heidelberg, svgdev
- XPert XRD tool (SNSF)

Characterization tools

- Woollam
- XPert XRD tool
- Electrical measurement tool
- SEM

Materials:

- p-type Si wafers (14)

RESULTS

The following samples were prepared using the Savannah ALD chamber in the order given:

1) 400 cycles, 25s purge, 200 °C
2) 400 cycles, 15s purge, 200 °C
3) 200 cycles, 15s purge, 200 °C -> forgot cover
4) 200 cycles, 25s purge, 200 °C
5) 400 cycles, 25s purge, 200 °C (repeat)
6) 300 cycles, 25s purge, 200 °C
7) 200 cycles, 25s purge, 100 °C
8) 400 cycles, 25s purge, 100 °C
9) 400 cycles, 15s purge, 200 °C (repeat)

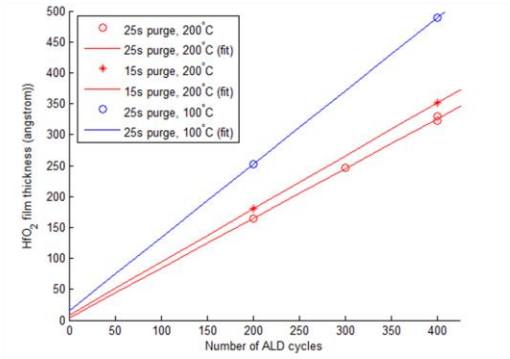
Note that samples 5 and 9 are a repeat of samples 1 and 2, respectively – the reason for the repeat being that a 15 second HF dip was initially incorporated between the SC1 and SC2 steps during the pre-ALD clean; however, it was realized that this does not yield a surface favorable to ALD nucleation. In subsequent depositions, the HF dip was not done.

A) Thickness vs ALD cycles

Fig. 1 shows how the film thickness, averaged from a 9-point Woollam measurement, varies with the number of ALD cycles. While measurements were done on both the films on Si (with the MOS devices, placed at the left side of the chamber) and thermal SiO_2 substrates (with the MIM devices, placed at the right side of the chamber). Note that the error in the measurement is higher for the SiO_2 devices, because the HfO_2 thickness could not be directly measured without estimating the thickness of the underlying SiO_2 film at each point. The points were then fit to a linear relationship to obtain, from the slope, the deposition rate and intercept. For the MOS devices, the deposition rate was around 0.80 Å/cycle for the devices deposited with a 25 s purge at 200 °C, and 0.86 Å/cycle for the devices deposited at 15 s purge. The slightly higher deposition rate for the shorter purge is within expectation, as this gives less time for excess precursor to be pumped out of the chamber. Nonetheless, both values are within the generally reported range of ALD rates for HfO_2 films. For both the substrates, the films deposited at 100 °C gave significantly higher deposition rates of ~1.18 Å/cycle. In fact, we see that the 200 cycle film deposited at 100 °C is slightly thicker than the 300 cycle film deposited at 200 °C. There is likely some CVD growth going on, and the lower temperature may contribute to more by-products and contamination being incorporated into the film.

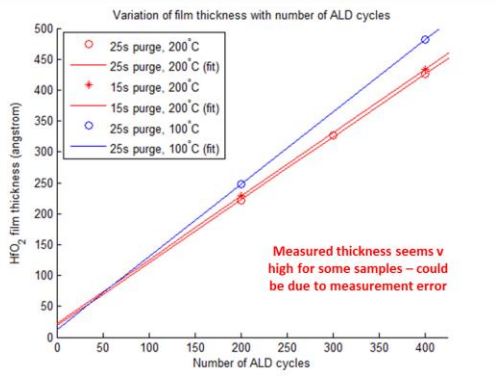
Fig. 1: Variation of film thickness with ALD cycles

MOS devices (L, Si)



Split	Slope	Intercept (Å)
25s purge, 200°C	0.804	4.295
15s purge, 200°C	0.857	8.660
25s purge, 100°C	1.185	16.670

MIM devices (R, SiO_2)



Split	Slope	Intercept (Å)
25s purge, 200°C	1.018	19.05
15s purge, 200°C	1.029	22.65
25s purge, 100°C	1.181	13.15

B) Scanning Electron Microscope images

Fig. 2a and b show SEM images taken for the samples before annealing. Immediately observable is the presence of light speckles on some of the samples, which ranged from around 5 to 30 nm in diameter. While a statistical analysis has not been done on this, it appears, as was previously noticed, that the density and average size of speckles for films deposited at 200 °C seems to increase in the following order: 200 cycle, 25 s purge → 200 cycle, 15 s purge → 300 cycle, 25 s purge → 400 cycle, 25 s purge

→ 400 cycle, 15 s purge. This is in the same order as the thickness of the films, so it can be inferred that density of speckles increases with film thickness, corroborating the model for development of crystallinity described in [4].

Two observations are worth noting here: 1) that there seems to be no significant effect of purge time (comparing splits 1 and 2, as well as 3 and 4) on the degree of crystallinity, and 2) that both the 200 cycle and 400 cycle samples deposited at 100 °C show very limited speckling. **This suggests that temperature, and not purge time (with the ranges used here) is the main factor contributing to crystallization in these samples.** It also suggests that decreasing the temperature would be an effective route to increasing amorphization, is the deposition rate were carefully calibrated.

Fig. 2a: SEM images – pre-anneal (Samples 1-4)

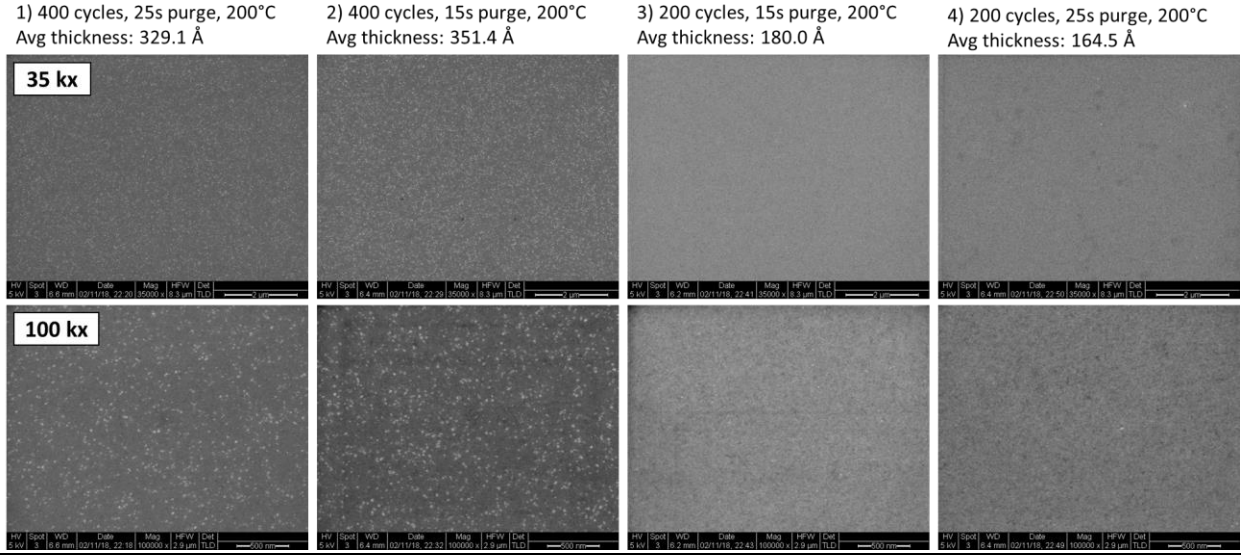
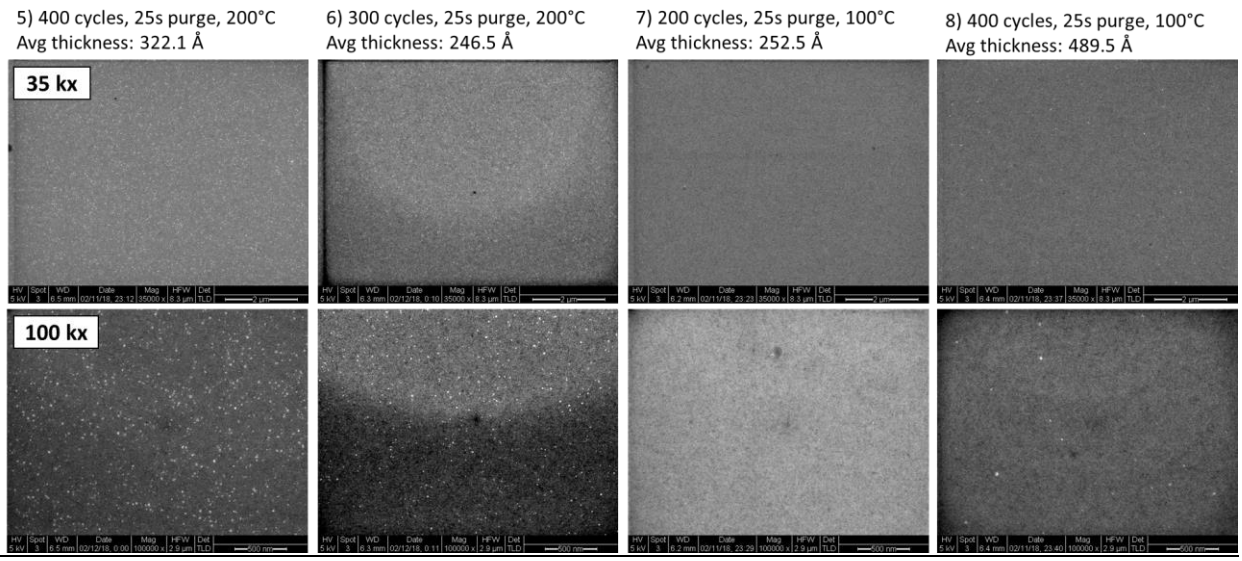


Fig. 2b: SEM images – pre-anneal (Samples 5-8)

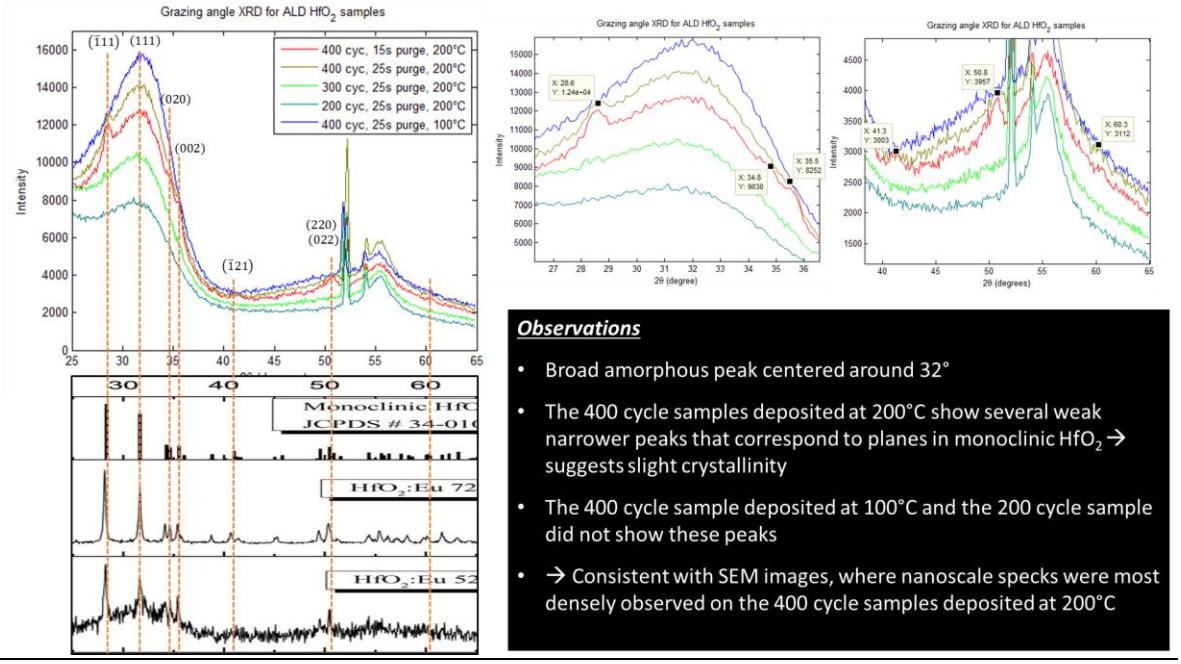


C) <u>X-Ray Diffraction measurements</u>

Grazing angle XRD measurements were done with between 25° and 65°. The sample size was 40 x 8 mm, and a slit size of 1/4° was used, with omega = 0.8°. XRD measurements on the films (Fig. 3) showed broad peaks centered around 32°, consistent with literature, and indicating that the films were mostly amorphous. The sharp peaks observed at ~52.4° can be attributed to the [311] orientation in the underlying Si (100) substrate. These features were present in all the samples studied. However, in

the 400 cycle samples deposited at 200 °C (and very slightly in the 300 cycle sample), we additionally observe a weak but narrower peak at around 28° (-111$_M$), 34.5° (020$_M$), 35.5° (002$_M$) and 41° (-121$_M$), 51° (220$_M$) and 60.5°. These do in fact correspond to the main peaks for monoclinic HfO_2, as can be seen from the comparison in Fig. 3. The fact that these peaks are only present for the thicker samples deposited at 200 °C and not the thinner ones, nor the ones deposited at 100 °C, aligns with the observations of speckles in the SEM images, and suggests that the weak peaks originate from the nanocrystallites. This observation is interesting as the deposition temperature here is relatively low, and the films are much thinner than the 100 nm samples for which the onset of crystallization was observed in literature.

Fig. 3: XRD measurements for selected samples



D) Capacitance-voltage measurements

Capacitance-voltage (C-V) measurements were done at 10 kHz, 100 kHz and 1 MHz before and after annealing on both the MOS samples (deposited on the left side of the chamber, and the MIM samples (deposited on the right side of the chamber). The voltage was swept from accumulation (-5V) to inversion (+5V) and back to accumulation again. The pre-anneal raw measurements for 10 kHz are shown in Fig. 4, and the capacitance density vs voltage measurements in Fig. 5. The MOS C-V characteristics yielded the typical sigmoidal shape for metal-oxide-semiconductor structures, with an accumulation region at negative biases, and depletion region where the depleted thickness of the semiconductor increases with positive bias, causing the capacitance to drop, and a region of deep depletion, where the capacitance approaches its minimum value. The only exceptions to this were the pre-anneal C-V characteristics for samples 1 and 2, which unlike all the other samples, were prepared with a HF dip to remove native oxide. For these samples, the C-V curves had a skewed U-shape, whereby deep depletion is not observed and the capacitance instead returns to its highest values at positive biases owing to channel inversion to create n-type carriers. The HF dip clearly has changed the interface behavior, though the mechanism for this has yet to be determined.

Another observation was that the anti-clockwise hysteresis in the C-V curves was around 0.5 V for the pre-anneal samples which were prepared without the HF dip, and much larger—~3V—for the samples 1 and 2, prepared with the HF dip. In both cases, the direction of flatband voltage shift going from the forward to reverse sweep was in the positive voltage direction. Flatband voltage shifts are associated with slow states in the oxide or at the interface which fill up as the gate is swept in one direction, but do not empty out fast enough as the voltage is reversed. (Note that if the flatband voltage shift were due to mobile charge instead, e.g. Na+ ions, we would expect the shift to be in the opposite direction, giving a clockwise hysteresis.) Charge trapping occurs if unsaturated bonds and/or vacancies are present, and can be passivated with an anneal. This is indeed observed, and in the second row of Fig. 5 we can see how the same samples after a 300 °C, 30 minute anneal exhibit much reduced hysteresis. Interestingly, samples 1 and 2 also no longer display a U-shaped C-V characteristic, but no have a sigmoidal one as well. However, the flatband voltages have also shifted closer to zero (most occur around -0.5 V), and the slight distortion of the C-V curve close to threshold voltage (whereby inversion occurs) has also been reduced, giving a more abrupt decrease in

capacitance towards inversion, indicating a more ideal MOSCAP, with fewer surface states and fixed charges after annealing. Samples 1 and 2 still feature a more negative flatband and threshold voltage than the other devices (between -1 V and -2 V). The limiting capacitance values (in accumulation mode) do not change much, however, indicating that the dielectric constant is not altered much by this annealing procedure.

Fig. 4: Raw C-V measurements, pre-anneal @ 10 kHz, 200 um devices. (100 kHz, 1 MHz data not shown)

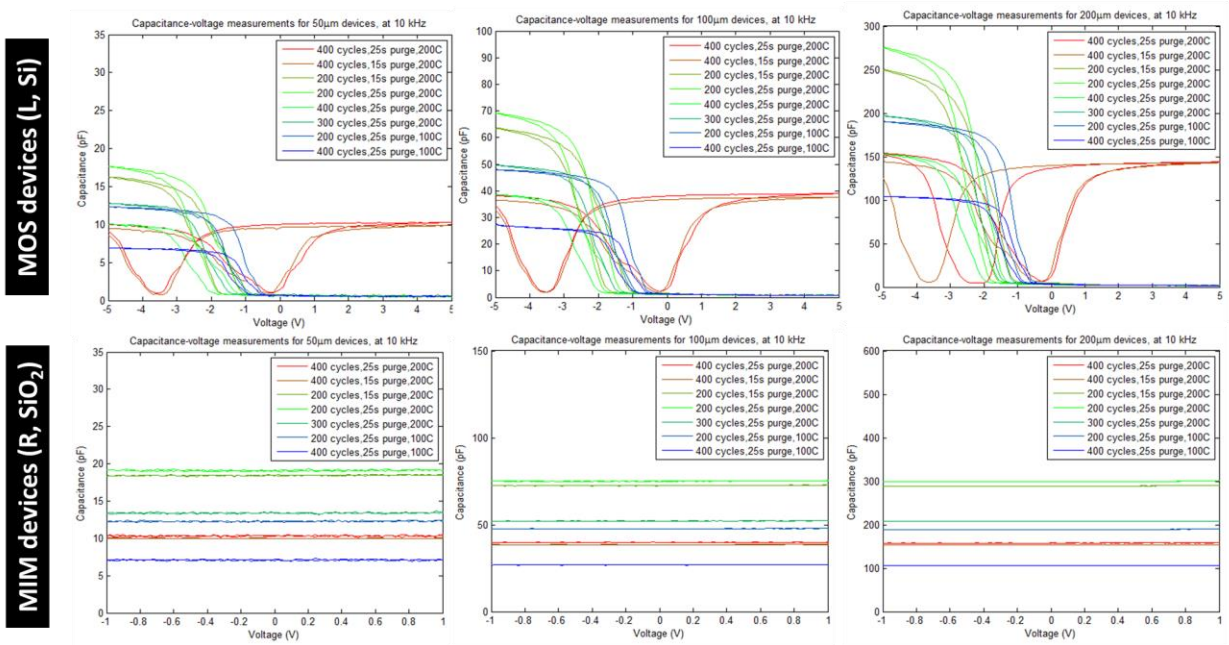
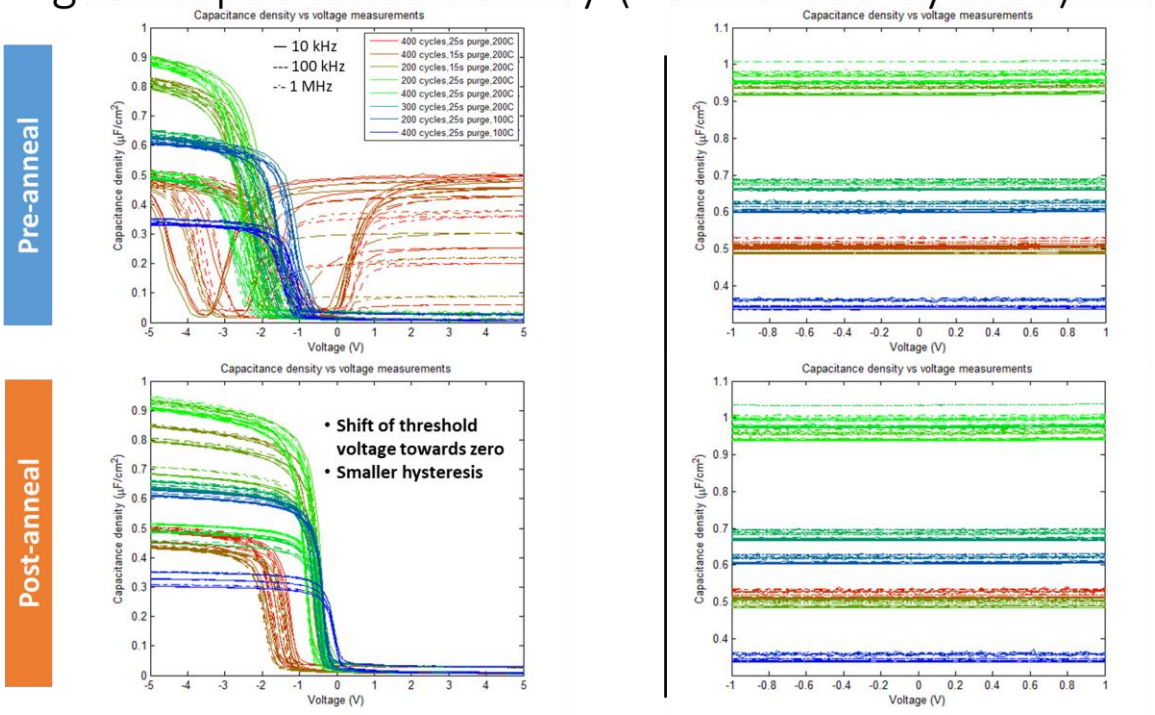


Fig. 5: Capacitance density (normalized by area)

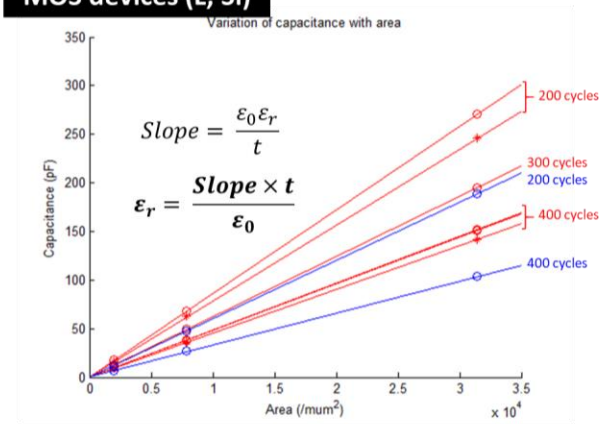


The MIM measurements yield a mostly flat C-V characteristic as expected. The capacitance values match those obtained from the MOS devices well, while being slightly higher in general (especially for the thinner films). This suggests a slightly thinner insulator region, and may be explained by the absence of a semiconductor layer which also contributes in a small amount to the capacitance of the MOS devices, due to its non-ideal properties as a conductor. This effect would be more noticeable in devices with thinner ALD films, where the thickness of the semiconductor capacitor is less negligible.

Fig. 6 plots the capacitance varies with device area. From this, the dielectric constant of the oxide can be estimated, using thickness measured on Woollam**. ε_r was found to average from ~16 to ~19**, which is within the expected range. The calculations for the MIM devices were done using thicknesses measured on their counterpart MOS devices instead, as the uncertainty here is expected to be lower. However, because of this there may be a systematic error on the calculated ε_r values. Interestingly, the ε_r values found from the MOS devices were on average lower. If we additionally account for the fact that the MIM devices, being deposited on the right side of the chamber, are expected to have slightly thicker ALD films than the MOS devices, we would get an even larger difference between the MOS/MIM ε_r values. This discrepancy may be partially explained by the fact that the thickness values measured on Woollam do not completely account for the insulator thickness in the MOS devices, due to the semiconductor. If this were the case, we would expect the actual dielectric constants of the MOS devices to be slightly higher than shown here.

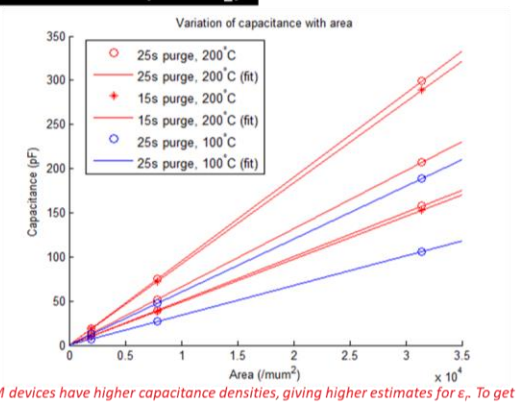
Fig. 6: Variation of capacitance with area (pre-anneal)

MOS devices (L, Si)



Sample	ALD cycles	Thickness (Å)	Purge time (s)	Temperature (°C)	Capacitance of 200 um device (pF)	C_vs_A: Slope	Dielectric constant (from slope)
1L-MOS	400	329.05	25	200	152.23	0.0048	18.00
2L-MOS	**400**	**351.4**	**15**	**200**	**142.07**	**0.0045**	**17.92**
3L-MOS	**200**	**180.03**	**15**	**200**	**246.11**	**0.0078**	**15.91**
4L-MOS	200	164.54	25	200	271.00	0.0086	16.02
5L-MOS	400	322.13	25	200	151.24	0.0048	17.49
6L-MOS	300	246.54	25	200	194.95	0.0062	17.26
7L-MOS	200	252.59	25	100	189.22	0.0060	17.17
8L-MOS	400	489.51	25	100	103.63	0.0033	18.20

MIM devices (R, SiO_2)

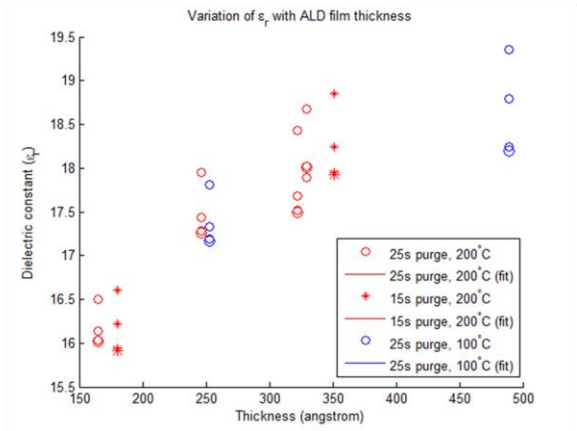


MIM devices have higher capacitance densities, giving higher estimates for ε_r. To get similar values as MOS devices, MIM insulators need to be ~92-95% as thick as quoted here.

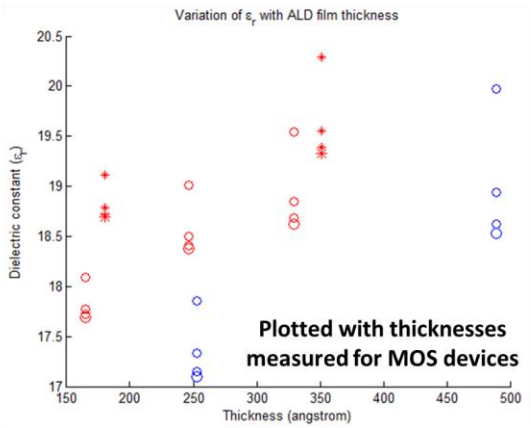
Sample	ALD cycles	Thickness (Å)	Purge time (s)	Temperature (°C)	Capacitance of 200 um device (pF)	C_vs_A: Slope	Dielectric constant (from slope)
1L-MOS	400	329.05	25	200	157.84	0.0050	18.62
2L-MOS	**400**	**351.4**	**15**	**200**	**153.42**	**0.0049**	**19.33**
3L-MOS	**200**	**180.03**	**15**	**200**	**289.06**	**0.0092**	**18.69**
4L-MOS	200	164.54	25	200	299.37	0.0095	17.69
6L-MOS	300	246.54	25	200	207.63	0.0066	18.37
7L-MOS	200	252.59	25	100	188.80	0.0060	17.10
8L-MOS	400	489.51	25	100	105.77	0.0033	18.53

Fig. 7: Plot of dielectric constant vs ALD film thickness (pre-anneal)

MOS devices (L, Si)



MIM devices (R, SiO_2)



The dielectric constants were plotted against the thickness of the films for which they were calculated in Fig. 7. This reveals a trend of (slightly) increasing dielectric constant with film thickness (though not necessarily in a linear way). Once possible explanation for this could come from what was observed in the SEM and XRD measurements—increasing crystallinity with increasing thickness. However, this does not fully explain why the samples deposited at 100 °C, for which a much lower density

of nanocrystallite speckles were observed compared to the 100 °C samples, pretty much lie along the same trend for the MOS devices. Another possible explanation is the dielectric constants were underestimated here, especially for the thinner films. In this case, the observed trend may just be an artifact. As a counterpoint to that, however, we note that we do also observe this trend with the MIM devices, for which this error is not relevant. Further studies would be needed to clarify this.

E) <u>Current-voltage measurements</u>

Current voltage measurements were done, by sweeping the voltage across the MIM devices from -0.5 V to 25 V while the current was measured. Plotted in Fig. 8 are the current density (current normalized by area) vs voltage (J-V) characteristics. The 1st column (a) shows the raw data with current density plotted on a log10 scale. The 2nd column (b) shows data that has been median filtered over an interval of 2 V to reduce noise, to allow the curves to be compared more easily. The 3rd column shows data that has been plotted on a log-log scale. In this visualization, the different regions of the characteristic become even more apparent. These include: I) a low bias region where the measurement is very noisy (as it is close to the noise floor), II) a roughly log-linear region of leakage current, followed by III) an abrupt increase to saturation, precipitated by breakdown of the insulator. In some cases, the current becomes unstable slightly before the shoot-up, suggesting a 'soft' breakdown.

Fig. 8: Current density vs voltage plots

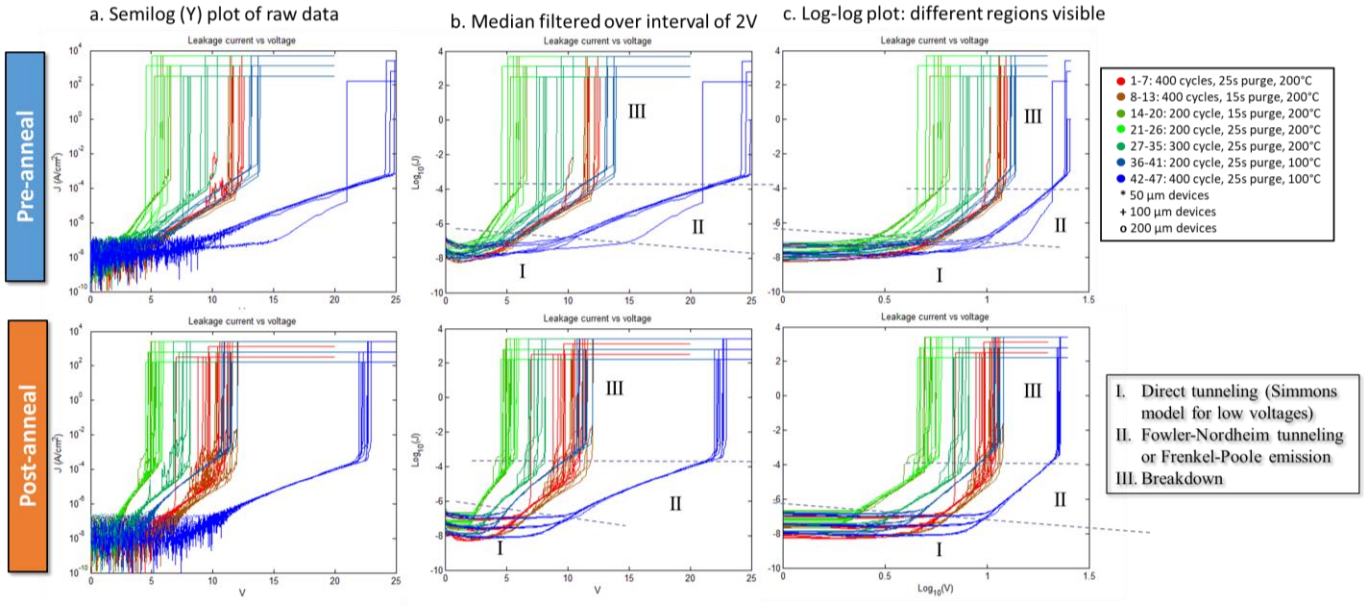


Fig. 9: Breakdown voltage vs film thickness

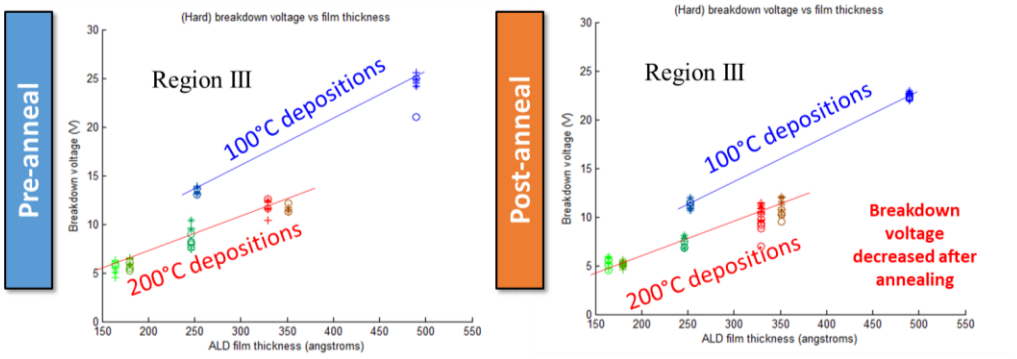


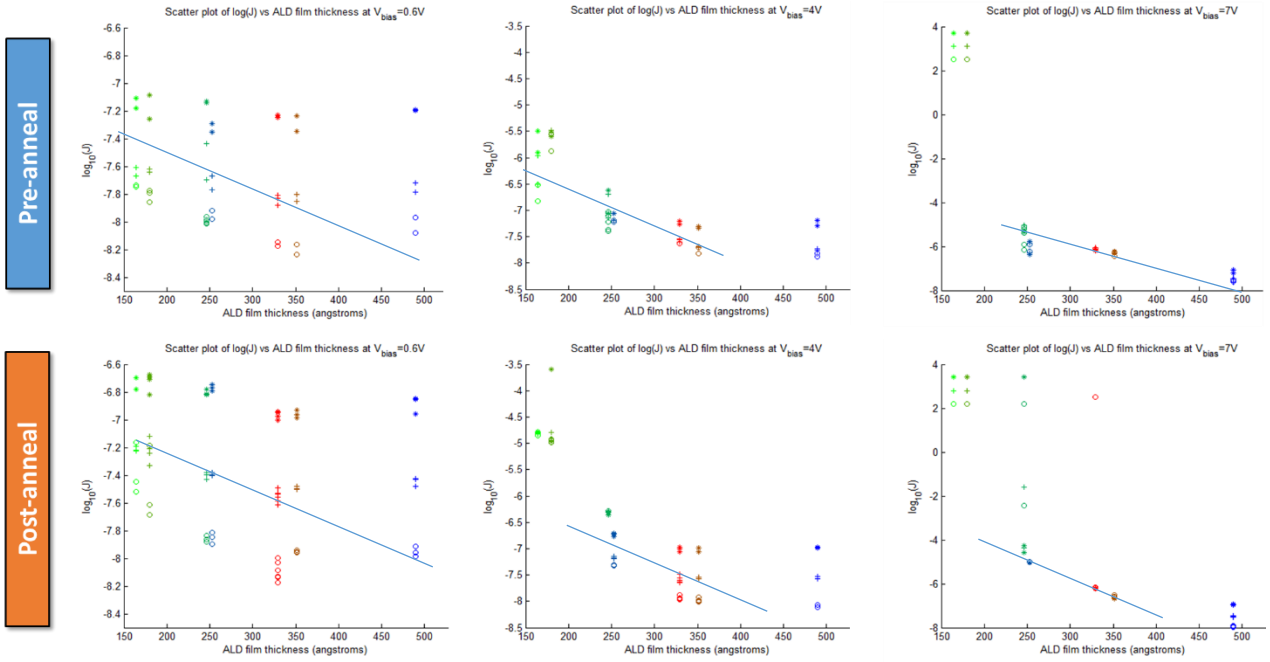
Fig. 9 plots the voltage at which hard breakdown occurs in the devices against the measured ALD film thickness. Dielectric strength is found to increase with decreasing film thickness, from about 3.6 MV/cm to 3.7 MV/cm for the pre-anneal samples deposited at 200 °C, and from 5.1 MV/cm to 5.5 MV/cm for the samples deposited at 100 °C.

After annealing, the breakdown voltages seemed to decrease slightly, ranging from 2.9 MV/cm to 3.3 MV/cm for the samples deposited at 200 °C, and from 4.3 MV/cm to 4.6 MV/cm for the samples deposited at 100 °C. These values fall within the reasonable range observed for HfO2 films in the literature.

Consistently, we see that the **films deposited at 100 °C have higher dielectric field strength**. This may mediated by the lower crystallinity that develops at this temperature, resulting in fewer grain boundaries that might facilitate degradation and breakdown and a higher breakdown field. This could happen because grain boundaries intrinsically contain a high density of defects which could cause more traps to accumulate, leading to the formation of a percolation path. This mechanism has been studied and reported in [8].

We also observe that dielectric strength decreases with annealing. One possible explanation that would also be consistent with the previous observation is that the annealing process could have caused some crystallization in the film, which in turn reduced the dielectric strength.

Fig. 10: Variation of current density (at 0.6, 4 & 7 V) with film thickness



Leakage current is generally higher after anneal

To compare the leakage current density for the different samples, the values at 3 voltage biases—(i) 0.6 V, (ii) 4 V and (iii) 7 V—were plotted against film thickness to observe relationships. There is a slight spread in the values for each sample, arising from the 3 different device sizes that measurements were taken from (*: 50 µm, +: 100 µm , o: 200 µm), and local inhomogeneities, etc. Nonetheless, at all 3 voltage biases, a general trend of decreasing current density with increasing film thickness is observed. Judging from the semilog(Y) plots in Fig. 10, we observe that this trend the dependence on thickness must be exponential in certain ranges at least, which is consistent with the thickness dependence in various tunneling current models. The data points that are anomalously high belong to devices which are on the brink of dielectric breakdown. It is worth noting though that the trendline that applies to the 200 °C samples in the above plots does not really seem to be shared by the samples deposited at 100 °C (turquoise and blue markers). The leakage current density for the 100 °C samples does not seem to be lower than that of the 200 °C samples, as one might expect from the higher dielectric strength of the films. In fact, the average leakage current density of the 400 cycle film deposited at 100 °C appears to lie above the trendline extrapolated from the 200 °C devices in all the plots. Finally, we observe that annealing also seems to increase the spread in leakage current density for all the samples.

To compare the current densities in the pre-breakdown regions (I and II) of the J-V characteristic, the data was further fitted to plausible models for current, and best fit slope parameter plotted against film thickness to observe trends. Region 1 (Fig. 11) is the low voltage region, extending up to roughly 1 V. Interestingly, the current density actually seemed to decrease slightly with increasing voltage in this region, resulting in a negative slope for the log-log characteristic. The explanation behind this observation is not entirely clear, and may have to do with the measurement limitations of the tool at ultra-low currents. Region 2 is the intermediate voltage region, extending from the end of Region 1 up till breakdown. 2 different models of leakage current are fitted—Fowler Nordheim tunneling (Fig. 12), which describes quantum mechanical tunneling across a triangular barrier, and Frenkel Poole emission (Fig. 13), which describes conduction in insulators where by a high density of defects results in traps close to the band edge, which dominate the current mechanism through a capture and emission process.

Fig. 11: Fitting region (I) to direct tunneling model

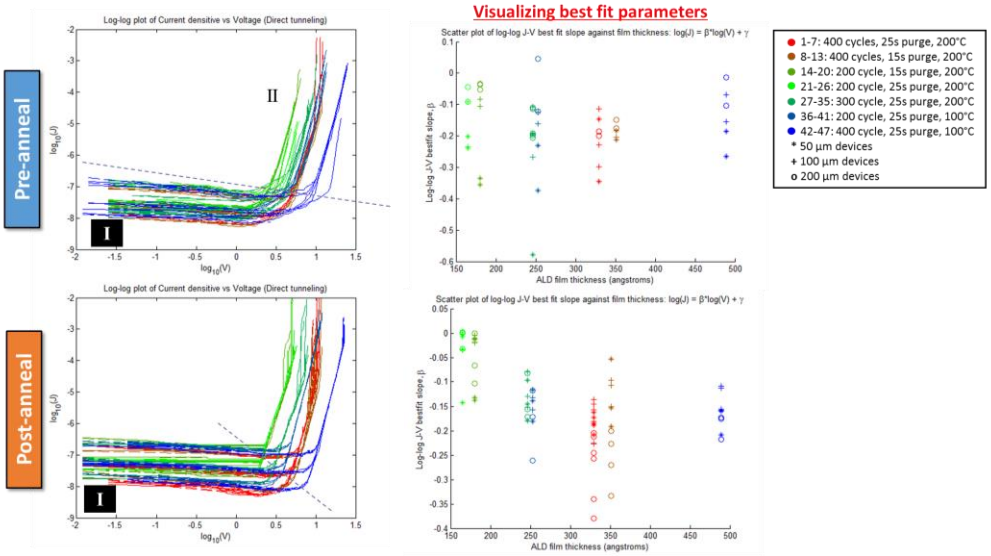
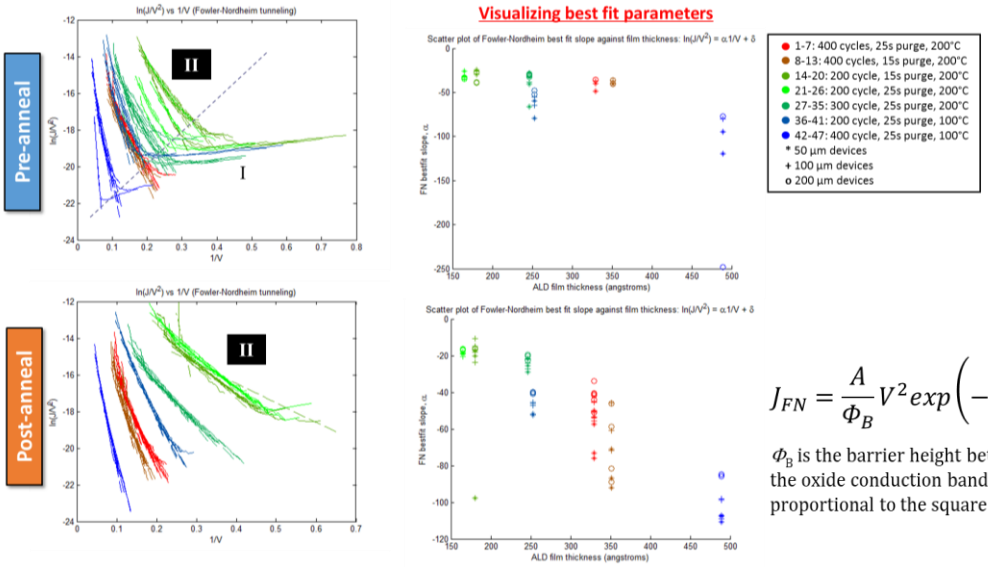


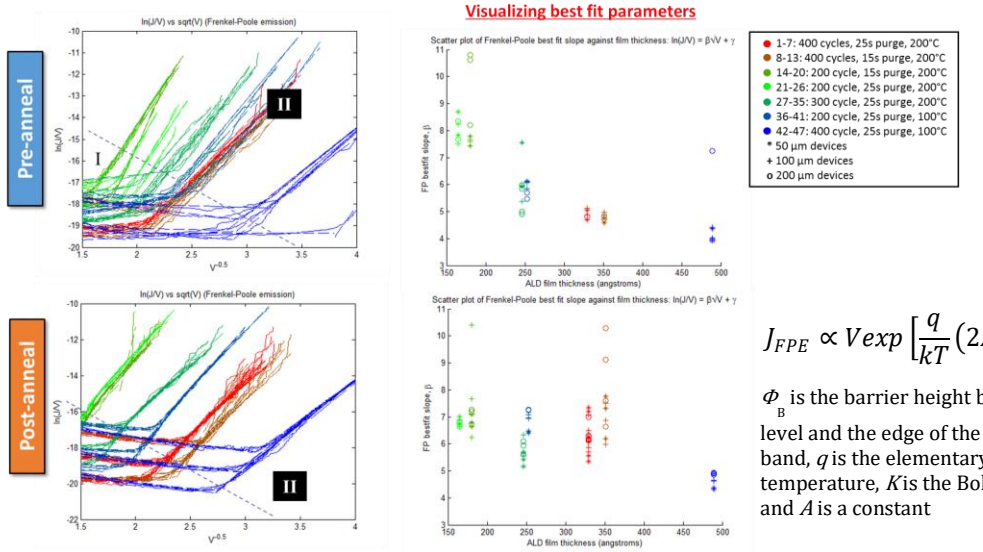
Fig. 12: Fitting region (II) to Fowler-Nordheim tunneling model



$$J_{FN} = \frac{A}{\Phi_B} V^2 exp\left(-\frac{B{\Phi_B}^{3/2}}{V}\right)$$

Φ_B is the barrier height between the metal Fermi level and the oxide conduction band, A is a constant, B is a constant proportional to the square root of the effective electron mass

Fig. 13: Fitting region (II) to Frenkel-Poole emission model



$$J_{FPE} \propto Vexp\left[\frac{q}{kT}\left(2A\sqrt{V} - \Phi_B\right)\right]$$

Φ_B is the barrier height between the trap energy level and the edge of the dielectric conduction band, q is the elementary charge, T is the temperature, K is the Boltzmann constant, and A is a constant

At first glance, both the Frenkel-Poole (FP) emission and Fowler-Nordheim (FN) tunneling models seems to give reasonably good fits to the data, although the FP fit seems slightly more linear. A statistical treatment, in conjunction with a literature review, would have been useful to evaluate this, but was beyond the scope of the present study. In addition to the slope, the y-intercept was also extracted from the plots. Together, these parameters may be used to estimate other values from the equations, for example the barrier height Φ_B and effective electron mass m_e.

F) Supplemental material on HfO2 / Al2O3 nanolaminate film

In addition to the HfO2 ALD splits reported above, a HfO2/Al2O3 nanolaminate film was tested as a way to suppress the development of nanocrystallites in the film. This was indeed observed—the nanolaminate film showed no roughness even under high SEM magnification. The deposition was done at 200 °C, with a 25 s purge between pulses. The recipe used was:

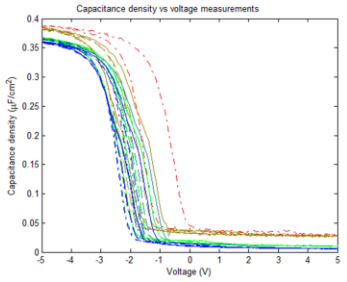
1: 5 cycles of Al2O3
2: 10 cycles of Al2O3
3: 10 cycles of HfO2
4: Steps 2 and 3 repeated 13 times
5: 20 cycles of HfO2

Based on the HfO2 deposition rate found earlier, assuming an Al2O3 deposition rate of around 0.9 Å/cycle, and assuming the dielectric constant of HfO2 to be 17.5 and that of Al2O3 to be 8, the equivalent HfO2 thickness was estimated to be around 413.5 Å. From the capacitance density plots from the MOS devices (see below), the apparent thickness of the film averaged around 420 Å, which is reasonably close. The apparent equivalent deposition rate for the nanolaminate film can be better calibrated with the aid of a 2 or 3 more depositions of different thicknesses.

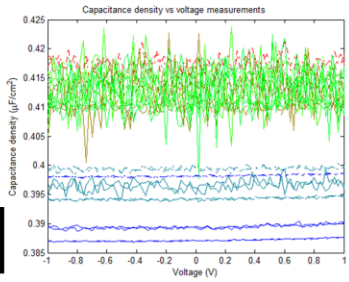
Fig. 14: Capacitance density vs Voltage plots for nanolaminate devices, and apparent equivalent HfO2 film thickness derived from measurements

Expected eq. thickness:
Assume ALD rates of
- 0.9 Å/cyc for Al2O3
- 0.8 Å/cyc for HfO2

➔ t_{eq} = **413.5 Å**



MOS devices (L, Si)



MIM devices (R, SiO_2)

Equivalent HfO2 thickness (Å) from measured capacitance density:
Assume $\varepsilon_{r,HfO2}$ ~ 17.5, $\varepsilon_{r,Al2O3}$ ~ 8

	50 µm_1	50 µm_2	100 µm_1	100 µm_2	200 µm_1	200 µm_2
10 kHz	400	425	402	427	400	423
100 kHz	405	431	407	433	404	425
1 MHz	424	431	426	433	423	426
Avg	*409*	*429*	*411*	*431*	*409*	*425*

➔ Pretty close to expected thickness

Apparent thickness of MOS devices: ~420 A

	50 µm_1	50 µm_2	100 µm_1	100 µm_2	200 µm_1	200 µm_2
10 kHz	372	375	375	377	371	373
100 kHz	375	391	378	393	374	388
1 MHz	375	398	377	400	373	389
Avg	*374*	*388*	*376*	*390*	*373*	*383*

MIM devices seem to have higher capacitance densities, giving rise to lower estimates for equivalent HfO2 thickness (~91% of MOS thicknesses)

The current density vs voltage data for the nanolaminate film is **plotted in black** alongside all the previous data in Fig. 15. Fig. 16 extracts the current density at 0.6 V, 4 V and 7 V. The leakage current density for the nanolaminate film appears to fall close to, if slightly above, the trendline extrapolated from the films deposited at 200 °C. There is no clear effect of annealing on leakage current.

From the breakdown voltage vs film thickness plots shown in Fig. 17, we observe clearly that the average dielectric strength of the nanolaminate film is significantly higher than the HfO2 films deposited at 200 °C. While there is some spread in the breakdown voltage value, which may be partly due to how the measurement was done (and possible film damage due to the probe), the dielectric field strength of the nanolaminate averaged around 4.7 MV/cm before annealing and 5.2 MV/cm after annealing. The increase in dielectric field strength after annealing is opposite to the effect observed with the HfO2 only films.

Fig. 15: Current density vs Voltage plots for all devices, nanolaminate data plotted in black

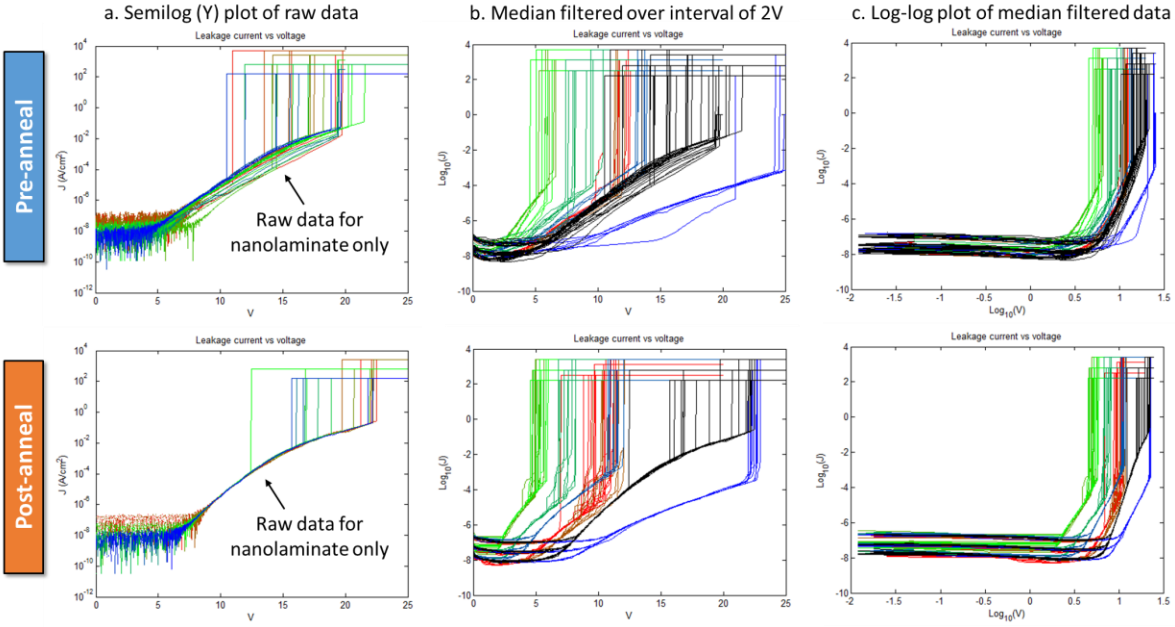


Fig. 16: Current density vs (effective) film thickness at 0.6 V, 4 V and 7 V

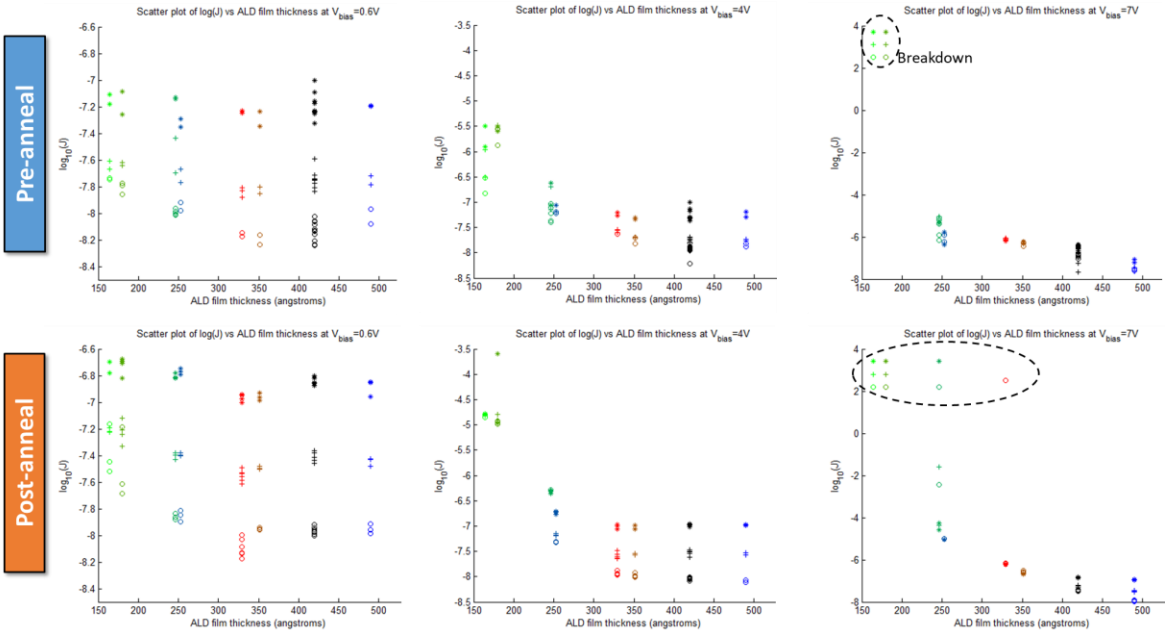
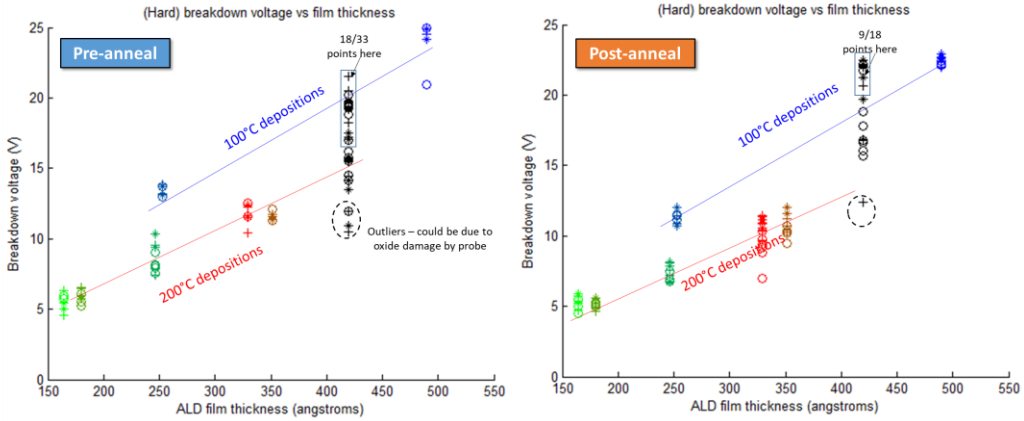


Fig. 17: Breakdown voltage vs film thickness before and after anneal



G) Summary

- SEM images show that the 400 cycle films deposited at 200 °C have a high density of bright speckles. There isn't much difference between the films deposited with 15 vs 25 second purge, so deposition time is not the limiting factor for the development of this morphology.
- Speckle size and density increases with the number of cycles. This is surprising as we aren't expecting very much crystallinity at all at 200 °C and < 40 nm thickness, when in fact we have a pretty rough-looking film.
- The 400 cycle film deposited at 100 °C shows only sparse speckles, even though it is thicker. Temperature seems to be the determining factor for morphology development in our samples.
- XRD measurements show that most of the films are amorphous, but a few peaks corresponding to monoclinic HfO2 can be discerned for the 400 cycle films deposited at 200 °C. This suggests that the roughness observed in SEM is related to a degree of crystallinity. The bright speckles may be nanocrystallites.
- Capacitance density vs thickness plot for both MOS and MIM devices suggests that dielectric constant increases with thickness(varying from ~16 to 19.5 within our sample range of 20 and 45 nm), though other factors (e.g. deposition temperature) may also contribute. This suggests that crystallinity is developing as thickness increases and causing the increase in dielectric constant, even if it's not directly detectable with SEM or XRD yet.
- In general, leakage current density varies exponentially with film thickness as expected. No clear effect of purge time or temperature on leakage current density.
- Breakdown voltage seems to vary linearly with film thickness in general, suggesting a roughly constant dielectric strength. However, the films deposited at 100 °C and the nanolaminate film seem to have slightly higher dielectric strength.
- Annealing at 300 °C for 30 mins does not have much effect on the dielectric constants, although it improves the shape of the C-V characterestics (i.e. reduces the threshold voltage and hysteresis).
- Annealing also seems to cause leakage current to increase slightly (especially at low voltages), and breakdown voltage to decrease by ~1V. The only exception was the nanolaminate film, which seems to see an increase in dielectric strength with annealing.
- Suggestions for future work:
    - It would be interesting to see the effect on morphology, dielectric constant, leakage current and dielectric strength of a higher temperature (e.g. 600 °C) anneal.
    - To improve the I-V measurements on the MIM devices, probe pads should be incorporated to avoid damage to the measured area of the film.
    - A more sophisticated error analysis should be performed to evaluate confidence in trends observed.
    - TEM measurements can be done to clarify the development of texture of the nanocrystallites.

REFERENCES

1) S. Gieraltowska et al, Characterization of dielectric layers grown at low temperature by atomic layer deposition, Thin Solid Films 577 (2015) 97.
2) S. Gieraltowska et al, Properties of thin films of high-k oxides grown by atomic layer deposition at low temperature for electronic applications, Opt. Appl. 43 (2013) 17.
3) J. Aarik et al, Texture development in nanocrystalline hafnium dioxide thin films grown by atomic layer deposition, Journal of Crystal Growth 220 (2000) 105.
4) D.M. Hausmann et al, Surface morphology and crystallinity control in the atomic layer deposition (ALD) of hafnium and zirconium oxide thin films, Journal of Crystal Growth 249 (2003) 251.
5) H. Kim et al, Effects of crystallization on the electrical properties of ultrathin dielectrics grown by atomic layer deposition, Appl. Phys. Lett. 82 (2003) 106.
6) M.-Y. Ho et al, Morphology and crystallization kinetics in thin films grown by atomic layer deposition, Journal of Applied Physics 93 (2003) 1477.
7) K. Smithe, Low-T, High-κ Dielectrics for Transparent and Flexible 2-Dimensional Electronics, SNF Wiki, EE 412 report (2015).
8) K. Shubhakar et al, Study of preferential localized degradation and breakdown of HfO2/SiOx dielectric stacks at grain boundary sites of polycrystalline HfO2 dielectrics, Microelectronic Engineering 109 (2013) 364.