Community service project proposal

Characterizing ALD HfO_2 based on different deposition conditions

Mentor: Michelle Rincon (weekly meetings to review progress)

MOTIVATION

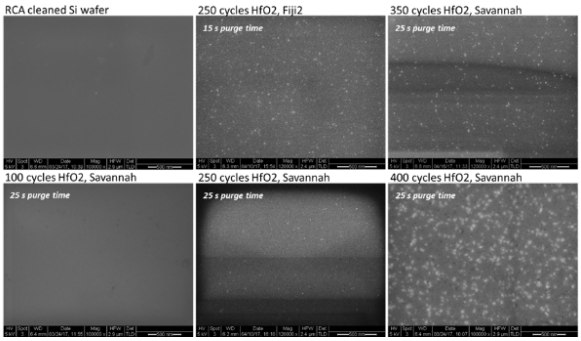


Fig. 1: SEM of ALD HfO2 films deposited at 200 °C

Recently, users have reported observing roughness in the form of 'hillocks' in thicker (> 20 nm) films deposited thermally in Fiji2 and Savannah at 200 °C. The hillocks seem to increase in size and density with the number of ALD cycles. Initial speculation is that they are nanocrystallites which nucleate over the long period of deposition, in spite of the low ALD temperature. This is surprising, as thin films of ALD HfO2 are expected to be amorphous at this temperature. Notably, the purge time between successive ALD cycles was increased from 15 s to 25 s around October 2015 to encourage self-limited growth, effectively increasing the process time by > 60%. It would be useful to see how film morphology varies with process time and temperature, as well as how it affects electrical properties. Amorphous layers are generally preferred for gate oxides due to lower leakage, although polycrystalline films may also be acceptable, and generally have the advantage of higher density and higher dielectric constant. Provided the resulting film is relatively smooth, polycrystalline films could still be used in capacitive applications if the crystallites in the film are much smaller than the film thickness so that grain boundaries do not extend through the thickness of the film, or if grain sizes are large and predictable relative to device feature size.

There are several studies in the literature that touch on the evolution of texture in ALD HfO2 films with temperature and film thickness. Gieraltowska *et al* report on a low temperature (T_g = 85 °C) recipe for HfO2 in the Savannah reactor, with TDMAH and DI water precursors and a purge time of 10 s. Table 1 shows the comparison of electrical properties of MOS structures based HfO2 thickness between 20 and 200 nm, deposited at 85 °C. In this case, the HfO2 films of thickness 100 nm and below were amorphous, with smooth surfaces (RMS roughness ~ 0.5 nm), and much lower leakage current and higher breakdown electric field than the crystalline film that developed at a thickness of 200 nm. At T_g = 135 °C, only the thinner films (20, 40 nm) were amorphous, and the 100 nm thick film was polycrystalline. The effect of deposition temperature on MOS capacitors formed with 100 nm thick films is shown in Table 2. As T_g increased, the degree of crystallinity, and consequently leakage current, dielectric constant and RMS roughness increased while dielectric strength decreased.

Table 1 (T_g = 85 °C)

Electrical properties and RMS roughness values of HfO_2 gate dielectrics grown at LT for five different thicknesses of insulator layers.

Thickness [nm]	Dielectric strength [MV/cm]	Leakage current at 1 V [A/cm^2]	Dielectric constant $k \pm 3$	RMS [nm]
200	0.6	$3*10^{-3}$	22	6.0
100	1.3	$2*10^{-6}$	21	0.5
80	1.2	$2*10^{-6}$	19	0.6
40	1.2	$8*10^{-5}$	15	0.4
20	1.0	$6*10^{-5}$	14	0.3

Table 2

Electrical properties and RMS roughness values of HfO_2 gate dielectrics grown at four different temperatures (T_G).

T_G [°C]	Dielectric strength [MV/cm]	Leakage current at 1 V [A/cm^2]	Dielectric constant $k \pm 3$	RMS [nm]
350	0.6	$2.4*10^{-3}$	18	2.9
200	0.6	$3.2*10^{-3}$	18	3.0
135	1	$8.2*10^{-4}$	17	1.6
85	1	$4.9*10^{-6}$	17	1.0

Fig. 2: The XRD determination of percent crystallinity as a function of deposition temperatures for 100 nm-thick hafnium and zirconium oxide films.

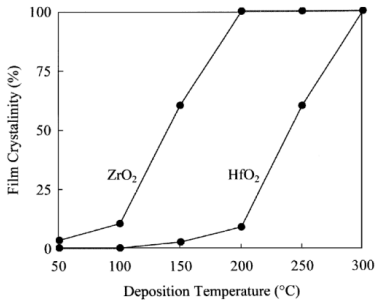
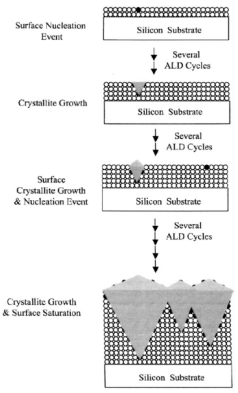


Fig. 3: Proposed crystal growth and nucleation model



Aarik *et al* deposited HfO2 films ranging from 30 – 375 nm using HfCl4 and DI water precursors, and a 2 s purge time. XRD and RHEED measurements demonstrated that films grown at 225 °C were amorphous, while polycrystalline films were obtained at 300 °C and higher, although at 300 °C the crystalline phase only appeared when more than 200 cycles were applied. The crystallite sizes were also observed to depend on the substrate material, being somewhat larger in the films grown on single-crystal silicon than in those grown on fused silica substrates. Hausmann *et al* deposited 100 nm thick HfO2 and ZrO2 films using TDMAH and TDMAZr at temperatures ranging from 50 °C to 300 °C, with 5 s purge time. For both materials, the degree

of crystallinity increased with temperature, as seen in Fig 2. HfO2 films deposited at 100 °C and below were found to be amorphous. TEM studies of 50 nm films revealed spherical and evenly distributed crystalline regions, which were correlated with roughness due to conical features in the AFM images. The roughness reached 5% of the film thickness for films deposited at 150 – 250 °C. Based on these observations, the authors proposed a nucleation and growth model for the ALD films starting with surface crystallite formation and faster vertical and radial growth of the crystallites compared to the surrounding amorphous material (Fig. 3). At higher growth temperatures, nucleation events become more probable and so films become more crystalline. For thicker films (> 100 nm), crystallinity starts to be observed at lower deposition temperatures because the longer process time allows more nucleation events and crystal growth to happen.

Kim *et al* found that ultrathin (3 nm) HfO2 films deposited at 300 °C were mostly amorphous, with sparsely distributed nanometer-sized crystallite 'seeds', but that significant crystallization resulted after a 30 minute anneal at 500 °C. Ho *et al* studied how annealing affects the degree of crystallinity of 20 nm thick HfO2 films deposited on p-Si substrates with a thin interfacial SiO2 layer grown either thermally or chemically (by rinsing wafers with O_3-enriched DI water). The ALD deposition was done with HfCl4 and DI water as precursors, at 300 °C. The HfO2 film deposited on thermal oxide was found to contain columnar grains of ~8 nm width, while the as-deposited film on the chemical oxide was mostly amorphous, though HRTEM imaging suggests short-range order on the sub-nanometer scale.

In his 2015 EE 412 report, Kirby Smithe described measurements done on MOSCAP devices made with ~10 nm of ALD HfO2, and a 15 s purge time. The Savannah depositions were done at 200, 150 and 100 °C and annealed in forming gas at 50 °C above deposition temperature, while the MVD depositions were done at 125 and 100 °C, and annealed at the same temperature.

Overall, the degree of crystallinity of the ALD HfO2 films seems to depend strongly on film thickness and deposition temperature, with some effect from the substrate. For *thin films* (< 40 nm) literature evidence suggests a deposition temperature of 200 °C should result in a mostly amorphous film (with similar ALD conditions, e.g. purge time), while crystallinity starts to be observed in as-deposited films around 250 – 300 °C. The effect of purge time has yet to be reported.

OBJECTIVES

To characterize the effect of 1) Deposition temperature, 2) Purge time and 3) Film thickness on the morphology and electrical properties of HfO2 films deposited in Savannah, before and after annealing. Deposition quality (thickness, uniformity, etc) will also be monitored.

SPLITS

1. 5 cycles Al2O3, **200 cycles HfO2**, 200 °C, 25s purge time
2. 5 cycles Al2O3, **300 cycles HfO2**, 200 °C, 25s purge time
3. 5 cycles Al2O3, **400 cycles HfO2**, 200 °C, 25s purge time
4. 5 cycles Al2O3, 200 cycles HfO2, 200 °C, **15s purge time**
5. 5 cycles Al2O3, 400 cycles HfO2, 200 °C, **15s purge time**
6. 5 cycles Al2O3, 200 cycles HfO2, **100 °C**, 25s purge time
7. 5 cycles Al2O3, 400 cycles HfO2, **100 °C**, 25s purge time

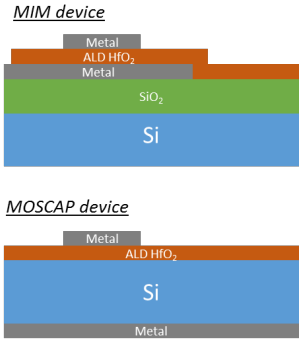


Fig. 1

SAMPLE PROCESSING

Each deposition will include a wafer for MIM devices, and another for MOS devices (cross sections shown in Fig. 1). A range of electrode sizes will be patterned ranging from 10 µm to 200 µm in diameter, which would allow extraction of both intrinsic normalized capacitance and parasitic capacitance from the capacitance-area plot.

MIM devices	***MOS devices***	***Time***	***Day***
• SC1 clean → SC2 clean	• -	1 h	1
• Grow 300 nm thermal oxide	• -	6 h	1
• *Measure oxide thickness with Woollam*	• -	0.5 h	1
• Photolithography to define 9-point testing sites	• -	2 h	2
• Deposit 5 nm Ti, 50 nm Pt as bottom electrode	• -	3 h	2
• Liftoff to remove metal from 9-point testing sites	• -	Overnight	2
• 10 min piranha clean	• SC1 clean → SC2 clean → HF dip	**1 h (x7)**	3-9
	• ALD deposition → *measure film thickness*	**4 – 6 h (x7)**	3-9

• ALD deposition → *measure film thickness* • Photolithography to define top electrodes • Deposit 5 nm Ti, 70 nm Pt or top electrodes • Liftoff • - • Cleave wafer in half • Anneal half of wafer • - • *Characterize electrical properties of devices* • *Characterize structural properties of devices*	• Photolithography to define top electrodes • Deposit 5 nm Ti, 70 nm Pt or top electrodes • Liftoff • Scratch backside oxide, deposit backside metal • Cleave wafer in half • Anneal half of wafer • *Characterize electrical properties of devices* • Dice wafer to obtain samples for XRD and SEM • *Characterize structural properties of devices*	2 h 3 h Overnight 3 h 0.5 h 0.5 h 12 h 3 h 5 h **Total time:** ~ 90 h	10 10 10 11 11 11 12 14 15 ~3 wks

The devices will be laid out on the wafers such that areas will be left 'empty', allowing a 9-point thickness measurement to be done to estimate deposition uniformity. This can be seen as the dark spots in Fig. 2. The grid of 1 mm squares indicates the positions individual devices. Half of the wafer is to be annealed while the other half is kept unannealed. Fig. 3 shows the placement of the device-carrying wafers and carrier half-wafers in the ALD chamber.

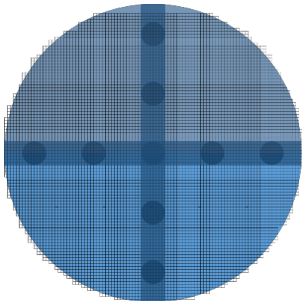


Fig. 3: Rough layout of individual wafer

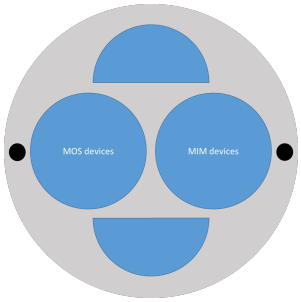


Fig. 4: Placement of wafers in ALD chamber

CHARACTERIZATION

Morphology:

- Woollam thickness measurement
- SEM imaging to visualize size and density of nanocrystallites (if present)
- AFM to characterize surface roughness
- XRD to characterize degree of crystallinity

Electrical characteristics:

- Leakage current and capacitance density can be obtained from MIM devices
- Capacitance density can also be measured from MOSCAP devices

TOOLS & MATERIALS

Device fabrication tools:

- Wbclean, wbsolv
- Thermco1
- Innotec (2 depositions)
- Savannah (7 depositions)
- Tylan9
- Svgcoat, Heidelberg, svgdev
- XPert XRD tool (SNSF)

Characterization tools

- Woollam
- XPert XRD tool
- Electrical measurement tool
- SEM
- AFM

Materials:

- p-type Si wafers (14)

REFERENCES

S. Gieraltowska et al, Characterization of dielectric layers grown at low temperature by atomic layer deposition, Thin Solid Films 577 (2015) 97.
S. Gieraltowska et al, Properties of thin films of high-k oxides grown by atomic layer deposition at low temperature for electronic applications, Opt. Appl. 43 (2013) 17.
J. Aarik et al, Texture development in nanocrystalline hafnium dioxide thin films grown by atomic layer deposition, Journal of Crystal Growth 220 (2000) 105.
D.M. Hausmann et al, Surface morphology and crystallinity control in the atomic layer deposition (ALD) of hafnium and zirconium oxide thin films, Journal of Crystal Growth 249 (2003) 251.
H. Kim et al, Effects of crystallization on the electrical properties of ultrathin dielectrics grown by atomic layer deposition, Appl. Phys. Lett. 82 (2003) 106.
M.-Y. Ho et al, Morphology and crystallization kinetics in thin films grown by atomic layer deposition, Journal of Applied Physics 93 (2003) 1477.
K. Smithe, Low-T, High-κ Dielectrics for Transparent and Flexible 2-Dimensional Electronics, SNF Wiki, EE 412 report (2015).