

ALD Dielectric Electrical Characterization

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Introduction

A pivotal part of transistors is their gate stack, and specifically the quality of the dielectric. The state-of-the-art research with transistors, ranging from highly-scaled silicon transistors, to germanium or III-V based transistors, to more novel devices such as carbon nanotube-based or MoS₂ transistors, all rely on the use of high-k dielectrics for increased electrostatic control of the channel. Thus high-k dielectrics are of utmost important for state-of-the-art device research within the SNF.

High-k dielectrics are most often deposited through atomic layer deposition (ALD). ALD is a highly controllable process, whereby a single atomic layer of the dielectric is deposited at a time. While this makes controlling the thickness of ALD films rather straight-forward, the suitability of these high-k dielectrics for transistor dielectrics is not as simple. In addition to just the thickness, the electrical properties of the dielectric (specifically the defects, locations of defects, and types of defects within the film) have huge implications on the final device performance. This project aims to shed light on the electrical properties of the most commonly used high-k dielectrics in the SNF.

While the ALD machines in the SNF are highly used, characterization data besides deposition thickness are not widely available. This leads individual lab members to conduct their own characterization runs, or simple to choose a high-k based on recommendations. Our goal is to provide some structure for future research to decide what high-k dielectric deposition machine and deposition method to pursue for their devices.

Methodology

To characterize the high-k dielectric films, we will use metal-oxide-semiconductor capacitor (MOSCAP) structures. A MOSCAP (shown below in Figure 1) is fabricated by depositing a dielectric on a semiconductor, followed by depositing a metal on the dielectric. Unlike a traditional capacitor with two metal plates sandwiching a dielectric, a MOSCAPs capacitance is frequency and bias dependent, and is an extremely useful and common tool for characterizing the electrical properties of a dielectric. Specifically, the quantity of traps within the dielectric, the frequency response of these traps, and the fixed charges (i.e. defects) within the dielectric can be measured with a MOSCAP CV curve. Our goal is to determine the best MOSCAP fabrication flow, hopefully resulting in the best flow for future transistor fabrication.

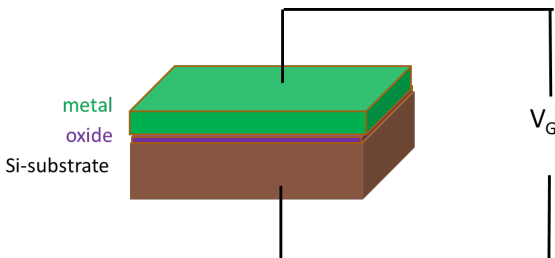


Figure 1: A standard MOSCAP. An oxide separates a semiconductor and metal, resulting in a frequency-dependent capacitance. The back-side of the Si-substrate can have a thick 100nm coating of aluminum for improved backside contact when measuring.

Experimental MOSCAP Variations

We will examine several different variations in MOSCAP fabrication to determine the best fabrication flow. We will vary the:

1) Dielectric

A significant unanswered question is what ALD machine produces the most defect and trap-free dielectric film. We will compare Fiji1, Fiji2, Fiji3, and Savannah, plasma versus thermal ALD, and Al_2O_3 and HfO_2 , using the standard recipes.

2) Gate metal

For all of the above films, we will do both evaporated and sputtered gate metals, to see which gate metal deposition method is most promising. We will use 90 nm Al, a common gate metal.

3) Annealing

We will sweep anneal temperatures in FGA to determine the ideal range for annealing the dielectrics. We will anneal in RTA2 at 250C, 300C, and 350C.

A graphical layout of the different MOSCAPs to be fabricated is shown below in Figure 2:

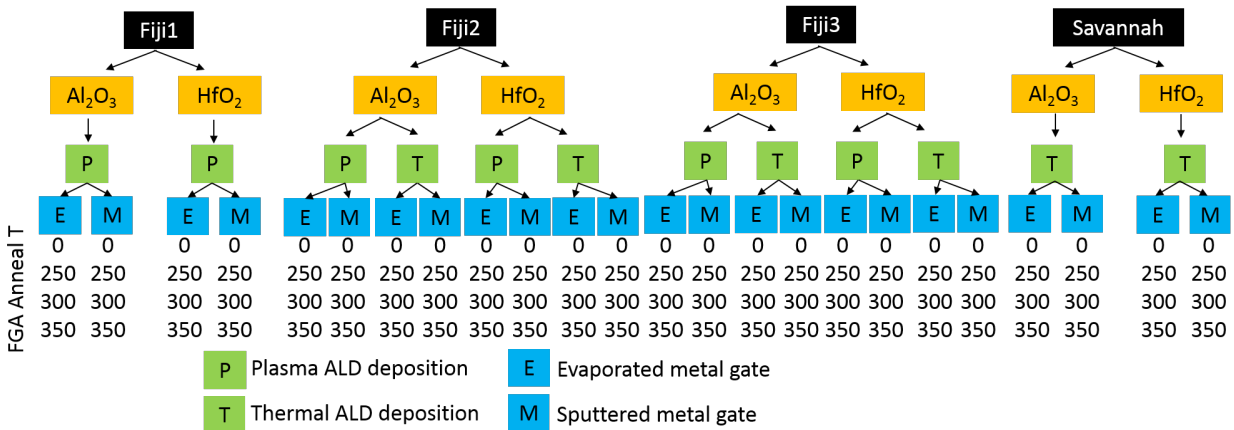


Figure 2: Schematic of all ALD films tests with MOSCAPs.

This graph shows every final MOSCAP fabricated, totaling 96 different MOSCAP types. We aim to have two deliverables:

1) Answer the following bigger-picture questions:

a) Is there a difference between the different ALD chambers? Is Fiji1, a clean chamber, higher quality than Fiji2, a gold-contaminated chamber? Is Fiji3 higher quality without any conductive films allowed inside? Is there a difference between savannah versus Fiji?

b) Is there a difference between thermal and plasma deposition films? Do plasma films really not inject charge into the oxide?

c) Should metal gates be evaporated in Innotec or sputtered in Metallica?

d) Is there an ideal FGA anneal temperature?

2) Raw data for labmembers to access: (this is a work in progress, to be continued over the summer, due to the large number of measurements needed on a busy measuring piece of equipment).

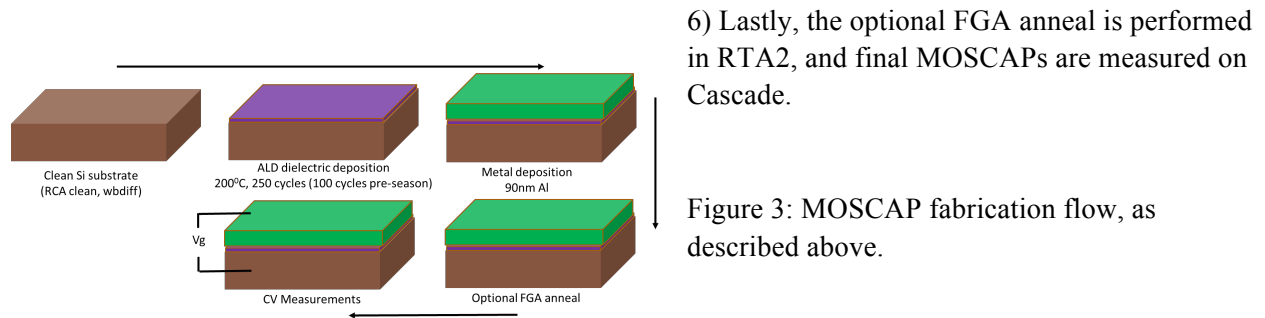
a) matlab .mat file with the CV curves for all of the 96 MOSCAPs.

b) the moscaps themselves for labmembers to check-out and measure or test for their processes as they see fit.

Process flow

The process flow is shown in Figure 3:

- 1) RCA clean bare silicon wafer immediately before loading into ALD chamber.
- 2) Make sure ALD chamber pre-seasoned with 100 cycles before actual deposition.
- 3) Run standard recipe of the dielectric to get desired thickness (200⁰ C).
- 4) Deposit metal gate (sputter or evaporate)
- 5) Pattern and etch metal for your pattern. For MOSCAPs, we pattern circular MOSCAPs, with 200 μ m radius, using 1 μ m 3612 and Karlsuss exposure.
- 6) Our gate metal is aluminum, so we follow the resist patterning with standard aluminum etchant. The photoresist is stripped in acetone and dried in IPA.



Results:

Plasma versus thermal:

Below are sample MOSFET curves for Al₂O₃, comparing both thermal and plasma ALD (Figure 4).

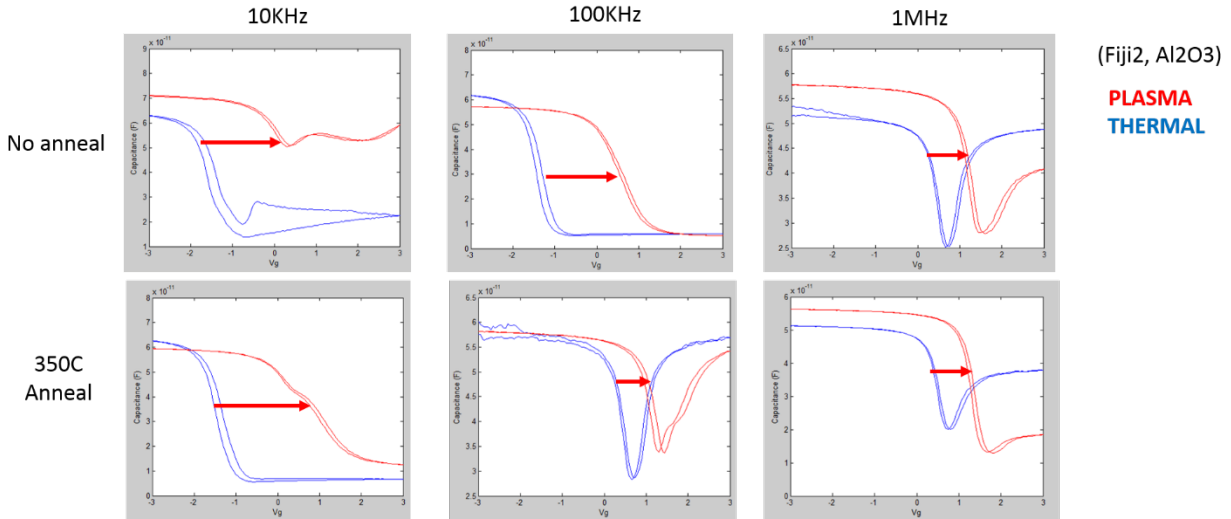


Figure 4: CV curves at a range of frequencies, both without and after 350C forming gas anneal.

There is a substantial difference between our thermal and plasma ALD. The plasma ALD results in a large positive flatband voltage shift, and a decreased subthreshold slope between accumulation and inversion. Importantly, the plasma ALD always results in more of a high-frequency response compared to the thermal ALD. All of these factors support that plasma ALD damages the interface, resulting in increased surface traps.

2) Metallica vs. Innotec:

The difference between metal deposition techniques, whether metallica or innotec, were 2nd order, and did not have a large effect on the MOSCAP performance. Sample CV curves for MOSCAPs fabricated with sputtered and evaporated aluminum as the top metal are shown below (Figure 5). The difference between the two cases are negligible.

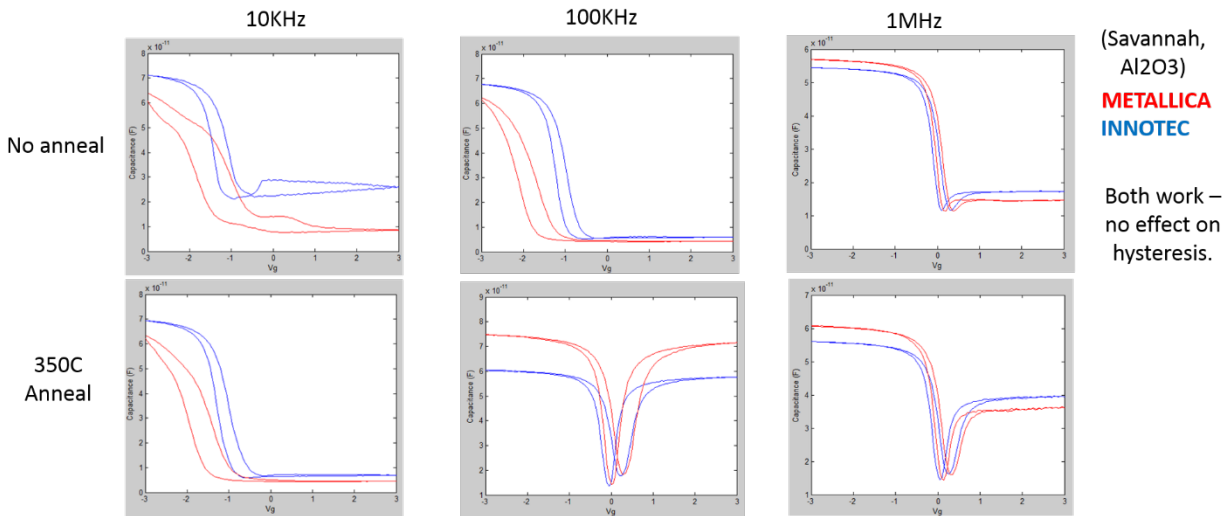


Figure 5: CV curves at a range of frequencies, both without and after 350C forming gas anneal.

3) Annealing temperature:

Annealing temperature in FGA (in RTA2) drastically improves the performance of the MOSCAPs, and thus should always be performed when possible. However, a higher temperature anneal is not always necessary, as any temperature above 250C results in similar CV curves (Figure 6). This might also be dependent on the metal gate used on for the MOSCAP.

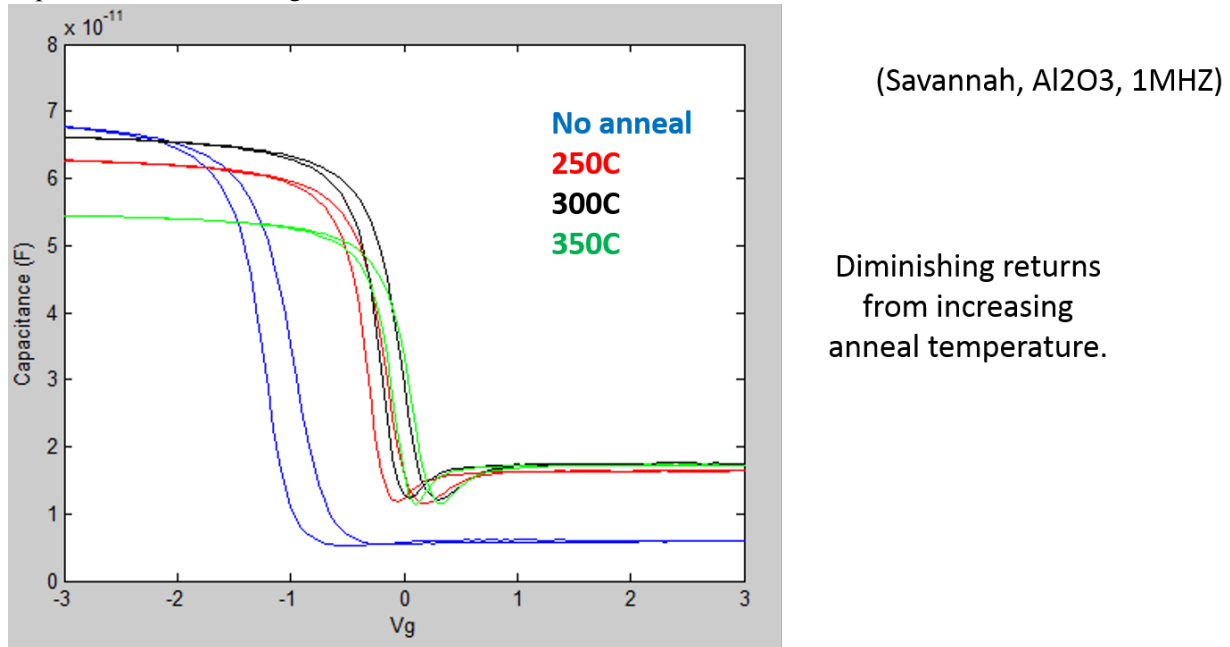


Figure 6: Typical CV curves showing trend of annealing temperatures versus the resulting CV curve.

4) Chamber:

Below show CV curves comparing Fiji1, Fiji2, and Fiji3 (plasma films), and Savannah, Fiji2, and Fiji3 (thermal films) (Figure 7). It is promising to see the majority of the films give reasonable CV curves. Fiji2 and Fiji3 give consistently good CV curves. Fiji1 has the least ideal MOSCAP results, with a hysteresis 5-6X larger than either Fiji2 or Fiji3. Even though Fiji1 is a clean chamber, the majority of usage is not dielectrics, unlike the rest of the chambers, which might account for the differences. Savannah, Fiji2, and Fiji3 all give reasonable CV curves for thermal films. Fiji3 is consistently the best performing dielectric.

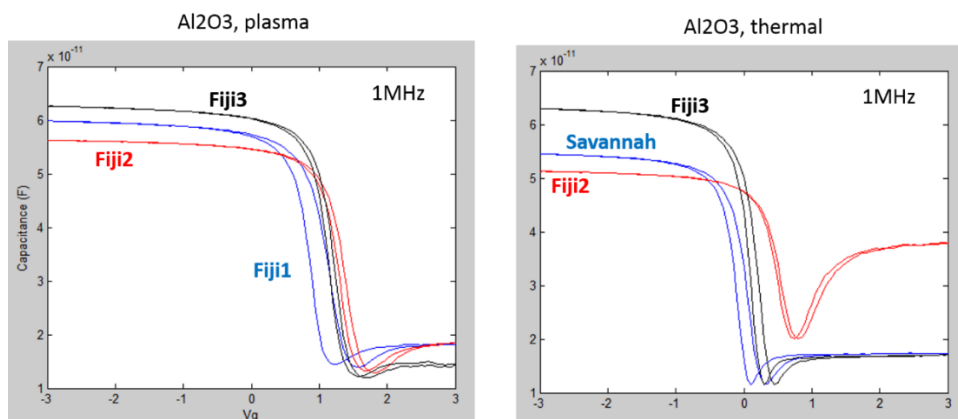


Figure 7: CV curves comparing all ALD machines within the SNF.

MOSFET fabrication:

In addition, we wanted to supply a standard NMOS process for use in the SNF, using the lessons learned from the MOSCAP work. Below is the detailed process flow for the MOSCAP fabrication, along with a sample IV curve, demonstrating reasonable $\sim 100\text{mV/dec}$ subthreshold slope. A simple n-type only process flow was chosen rather than a full CMOS flow due to the ease of processing associated with only one type of transistor. Isolation between transistors, such as through a LOCOS process, is not necessary, and the processing steps for the transistor fabrication (such as well doping) are 1/3 as many. For many users, a single type of transistor is sufficient for testing new dielectrics, gate metals, or mobility enhancers.

The process flow for the NMOS process is shown in Figure 8-9.

Step	Machine	Details	Notes
Clean	Wbnonmetal+wbdiff	Regular RCA clean	Use I-prime p-type wafers. $\sim 1e17$ doping for p-type channel
SiO ₂ growth	Thermco1,2,3,4	22nm dry oxidation, 900C	Measure thickness after with woolum
Pattern source/drain n-type implantation regions	PR coating (svgcoat) PR exposure (ASML) PR develop (svgdev)	3612, 1um resist. No hard-bake required.	This channel length is 2um.
N-type source/drain implantation	Outsource	Phosphorous, $1e15$ dose, 60keV. Energy depends on actual SiO ₂ thickness. This dose for 22nm yields $\sim 60\text{-}80\text{nm}$ junction depth.	
Resist strip	Gasonics	Regular recipe (3) for 1um 3612.	Optional wbnonmetal clean. Do NOT do HF dip, SiO ₂ must be intact for flash annealing.
Flash anneal	RTA-left	1050 in argon for 5 seconds	
Strip SiO ₂	Wb-flexcorr1-4	2% HF dip, 5	

		minutes.	
ALD Deposition	Savannah ALD	Al ₂ O ₃ , 200C, 125 cycles	Deposit ALD as soon as possible after SiO ₂ stripping in HF.
Pattern Source/Drain contacts	Headway (lol2000) Svgcoat (3612 1um) ASML (expose, 55 dose) Develop (program 5)	Headway: 3000 RPM, bake in oven at 195C for 22 minutes.	
Etch source/drain contacts	Wb-flexcorr1-4	2% HF, 50 seconds	Optional oxygen descum in drytek4. (I did both ways, saw no difference. More robust with the descum though)
Deposit source/drain contact metal	Innotec	5nm Ti/30nm Pt	
Lift-off	wbsolvent	Lift-off in acetone Remover PG for 15 minutes to remove LOI2000. Clean with IPA.	
Pattern gate	Headway (lol2000) Svgcoat (3612 1um) ASML (expose, 55 dose) Develop (program 5)	Headway: 3000 RPM, bake in oven at 195C for 22 minutes.	Optional oxygen descum in drytek4. (I did not do)
Evaporate gate metal	Innotec	5nm Ti/30nm Pt	
Lift-off	wbsolvent	Lift-off in acetone Remover PG for 15 minutes to remove	

		LOI2000. Clean with IPA.	
Optional: Passivation	Savannah ALD	10 nm Al ₂ O ₃ .	Need to re-etch contacts to source/drain. Used to covered exposed regions of source/drain due to undercutting of oxide to pattern source/drain contacts.
Anneal	RTA2	FGA anneal, 300C, 5 minutes	

Figure 8: Detailed process steps for NMOS fabrication.

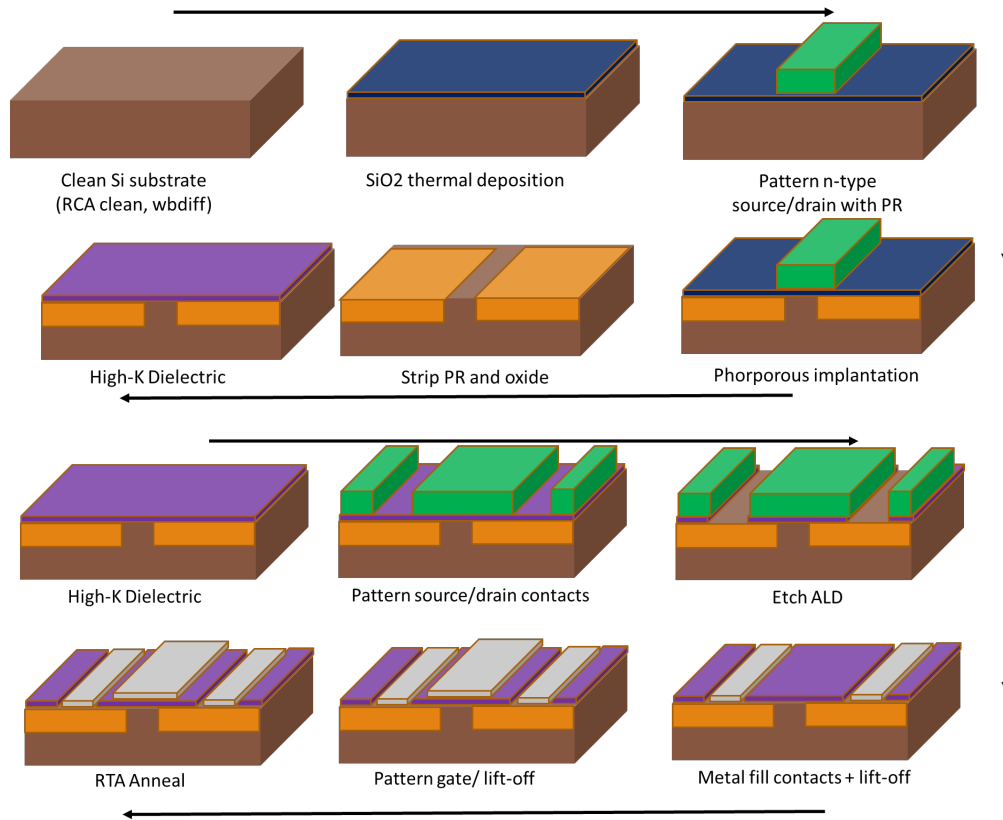


Figure 9: Process flow schematic for NMOS fabrication process.

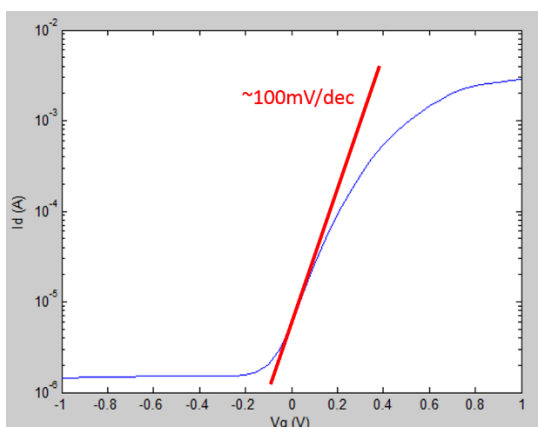


Figure 10: ID-VG curve for typical NMOS device. Reasonable device characteristics are observed.

Summary:

We investigated the electrical properties of every possible deposition method for the most common dielectrics used in the SNF: Al_2O_3 and HfO_2 . We also investigate different processing parameters for MOSCAP fabrication. Labmembers will have a database of MOSFET curves to download and analyze if they are interested, in addition to being able to use our pre-fabricated MOSFETs to test out processing steps. Given our data, we can answer some key questions:

- 1) Plasma ALD results in a degraded interface compared to thermal ALD and a positive flatband voltage switch.
- 2) Sputter and evaporated metal both work as gate metals on dielectrics, with little difference between the two.
- 3) RTA annealing can be performed at lower temperatures (250C) without sacrificing dielectric quality.
- 4) Fiji3 yields the nicest dielectrics, while Fiji1 the worst. Savannah and Fiji2 also yield nice dielectrics, somewhere between Fiji3 and Fiji1.

Additionally, we provide a baseline NMOS fabrication process for labmembers.