SNF Community Service Proposal for ALD Oxide Film Characterization

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The expanding flood of data generated by mobile devices and embedded systems has created a pressing demand for more robust electronic information storage to replace magnetic storage. Resistive random access memory (RRAM) is a promising alternative due to its energy efficiency, scalability, and multi-level operation. Here at Stanford, there is a major initiative by multiple groups (Wong, Wong, Nishi, and Fan) to develop a deeper understanding of and control over the cell filament formation process within the context of solid electrolyte materials, defects, and electrical lead geometries.

Metal oxide RRAM cells consist of a thin layer of metal oxide, such as TiO_2 or HfO_2, sandwiched by two metal contacts. When an electrical field is applied by the metal contacts to the oxide layer, oxygen anions can diffuse via "soft breakdown," leaving vacancies that can support electrical conduction. Through this process, the resistance between the electrodes can be controlled across multiple orders of magnitude. It is therefore essential, during cell fabrication, to deposit high quality, pinhole-free metal oxide layers that can sustain controllable and reversible soft breakdown processes. Atomic layer deposition (ALD) is a deposition technique that can produce high quality, thin film metal oxide layers, and is therefore used in academia and industry to fabricate RRAM devices.

Unfortunately, at the SNF, the quality of RRAM devices fabricated in-house has substantially deteriorated. An example is illustrated in Figure 1, where devices were tested by applying a series of voltage pulses, followed by resistance measurements (Figure 1a). In November 2013, the devices worked properly: they displayed gradual increases in resistance as a function of pulse number, which is as expected (Figure 1b). However, in February 2014, the devices displayed resistances that varied erratically as a function of pulse number. Since then, other groups (Wong and Fan groups) have attempted to make HfO_2 RRAM cells, and in all attempts, the devices did not cycle under DC sweeps. While there are many potential variables in the fabrication line that may contribute to device degradation, ALD film quality is suspected due to its potential variability in film quality, compared to other steps (i.e. lithography, metal deposition, etc).

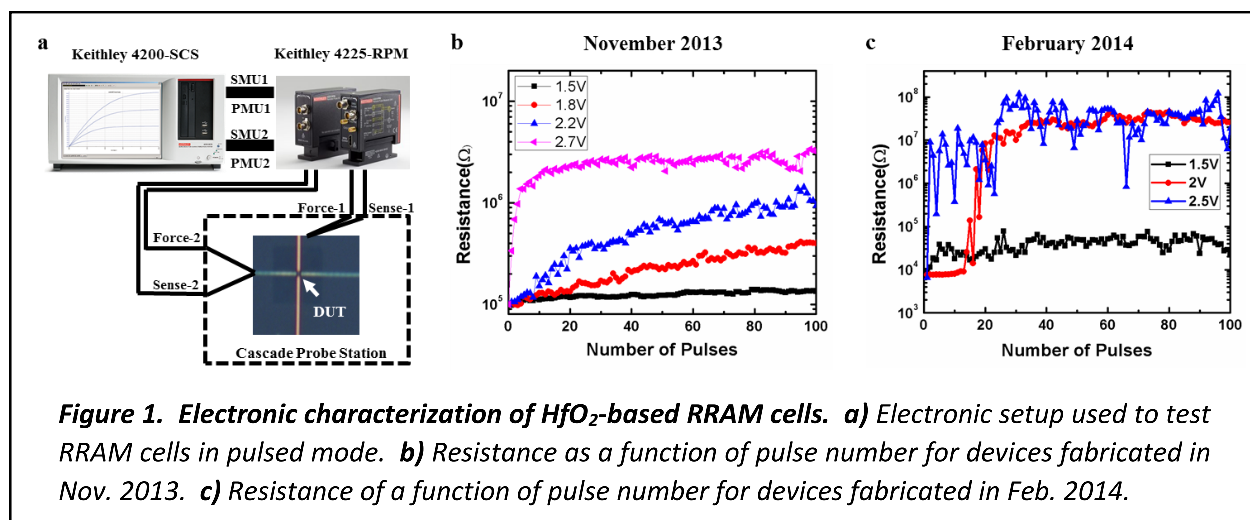

Figure 1. Electronic characterization of HfO_2-based RRAM cells. a) *Electronic setup used to test RRAM cells in pulsed mode.* ***b)*** *Resistance as a function of pulse number for devices fabricated in Nov. 2013.* ***c)*** *Resistance of a function of pulse number for devices fabricated in Feb. 2014.*

We propose to perform a **systematic analysis** of the **electronic properties** of ALD-based HfO_2 thin films in order to: 1) identify any variability in the ALD growth process in fiji2, fiji3, fiji4, and the Savannah that may contribute to RRAM performance degradation, and 2) develop a protocol for calibrating and evaluating thin oxide films on a regular basis to ensure the tool is properly used and maintained long term. This analysis builds on the *status quo*, which has been to evaluate the quality of oxide films optically by ellipsometry, by testing directly the dielectric breakdown properties of the oxide films.

In order to characterize the metal oxide thin films while eliminating as many variables from the fabrication workflow as possible, we propose three sets of devices to be fabricated. They are:

1) Pt/HfO_2/Pt hard breakdown devices using a common ground electrode and simple 100x100µm top electrode geometries. Here, inert Pt contacts are used on both sides to eliminate any variability incurred by the top titanium nitride metal contact. The hard DC breakdown of multiple devices (10's) will be tested and compared.
2) Pt/HfO_2/TiN RRAM devices using a common ground electrode and simple 100x100µm top electrode geometries. Here, TiN top contacts are used so that the devices can be cycled in soft breakdown mode. The IV curves of multiple (10's) devices will be measured and compared.
3) Pt/Al_2O_3/HfO_2/TiN RRAM devices using a common ground electrode and simple 100x100µm top electrode geometries. Here, a thin alumina layer will be deposited to ensure oxide wetting on the inert platinum bottom electrode. The IV curves of multiple (10's) devices will be measured and compared.

A summary of the detailed workflow for all of these devices is as followed:

1) Silicon wafers will be cleaned using standard cleaning process.
2) 30 nm Platinum will be deposited on the wafers by e-beam evaporation with Innotec.
3) Wafers will be put *immediately* without any wait into fiji2, fiji3, Savannah or fiji4 for an ALD process. 5 nm HfO2 will be deposited on the wafers (and in the case of device set (3), 5 cycles of Al_2O_3 will be initially deposited).
4) Photolithography will be *immediately* performed without any wait to define the top electrode patterns. Either 30nm Pt deposition with the Innotec or 30nm TiN deposition with the AJA in Prof. Wong's lab will be performed to define the top electrode material.
5) After lift-off, I-V curves of the devices will be tested using the Cascade Probe Station. The silicon substrate will serve as a bottom electrode during the measurements.

The work will be divided up by students from the Fan, Wong, and Nishi groups, and they will meet every 2-3 weeks with Prof. Fan, Michelle Rincon, Jim McVittie to understand and interpret their findings.